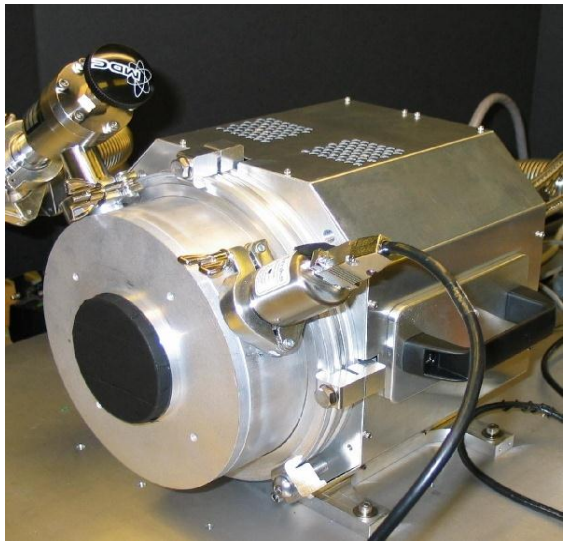
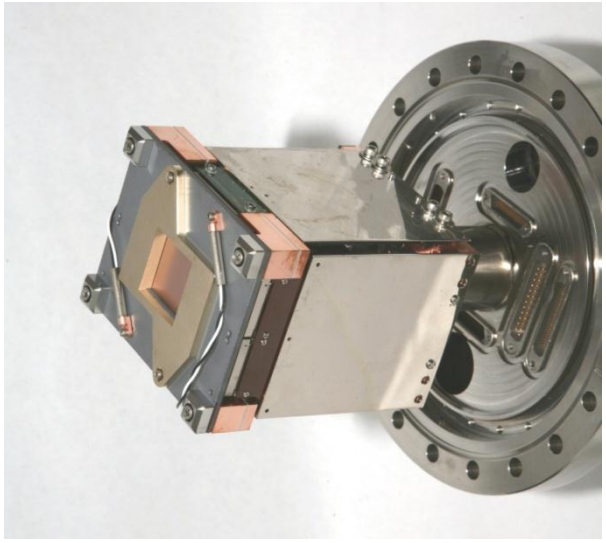
# Fast CCD X-ray Detector Collaboration with LBNL



480 Fast CCD Detector



1K Frame Store CCD

By: John Weizeorick

Date: 4-17-2012

# CCD X-ray Detector Collaboration with LBNL

- History of Fast CCD Detector Collaboration
- 1st Generation Fast CCD Detector
  - 480 Fast CCD Detector at ANL
  - 480 cFCCD Detector at LBNL
  - Status
- 2nd Generation Fast CCD Detector
  - 1K Frame Store CCD Design (1KFSCCD)
  - Status
- 3rd Generation Very Fast CCD Detector
  - Fully Column Parallel CCD

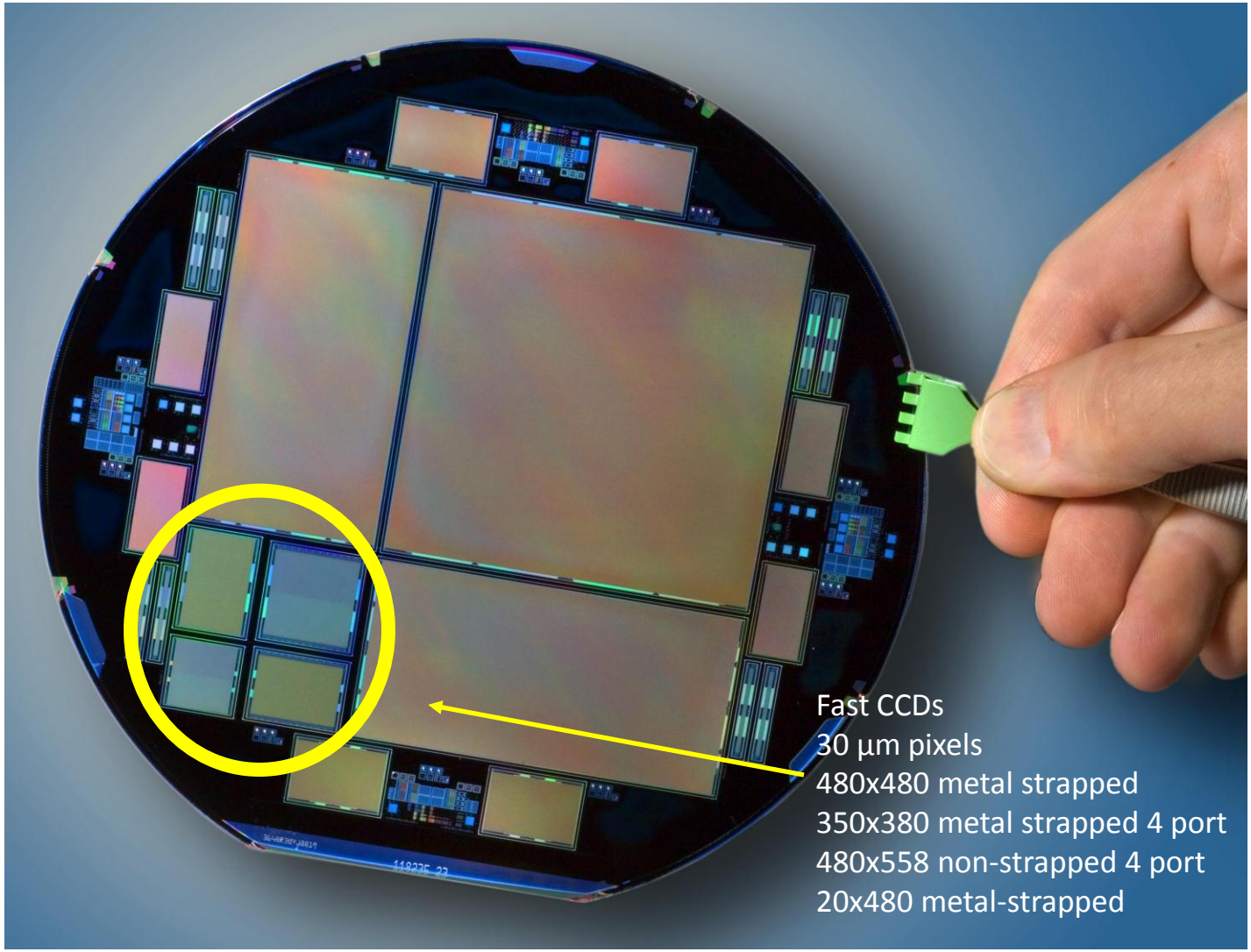
# History of Fast CCD Detector Collaboration

- SNAP - (Supernova / Acceleration Probe) – Proposed space based telescope
- SNAP CCD
  - CCD Mosaic camera ( half-billion pixel imager)
  - Being Developed by Custom Integrated Circuits group at LBNL lead by Peter Denes
  - SNAP Readout IC - LBNL
  - Thick, (>200 µm), Fully depleted, back-illuminated CCD imager
- Howard Padmore (ALS) and Peter Denes at LBNL
  - Realized SNAP CCD has characteristics that are useful for X-ray CCD
    - Back-illuminated – Higher optical quantum efficiency
    - Thick – Has enough mechanical structure that it can be used with a fiber optic taper, and can be used for direct x-ray direct.
  - Bought space on SNAP wafer run to build a 480 Fast CCD
  - SNAP CCD modified to achieve faster readout (almost column-parallel)

# History of Fast CCD Detector Collaboration

- SPIE Conference 2005 (International Society for Optical Engineering)
  - Howard Padmore gave talk “Fast CCD-based systems for detection of x-rays and electronics” H.A Padmore, C.J.Bebek, M.Church, P.Denes, C.R.M.Greaves, S.E.Holland, H. von der Lippe, Lawrence Berkeley National Lab
  - Steve Ross attended talk and meet with Howard after presentation
  - Discussed the possibility of collaborating with LBNL in the development and fabrication of x-ray detectors based on these fast readout CCD chips.
- 2005 Meetings with LBNL in October and December
  - LBL has expertise in IC design
  - ANL has expertise in design and fabrication of CCD-based x-ray detectors especially in the opto-mechanics and data acquisition electronics
  - Sent out letter to beamline scientist and users to get input and verify interest
  - At end of these meetings it was agreed that we would work together on developing a Fast CCD x-ray detector based on LBNL’s CCD.

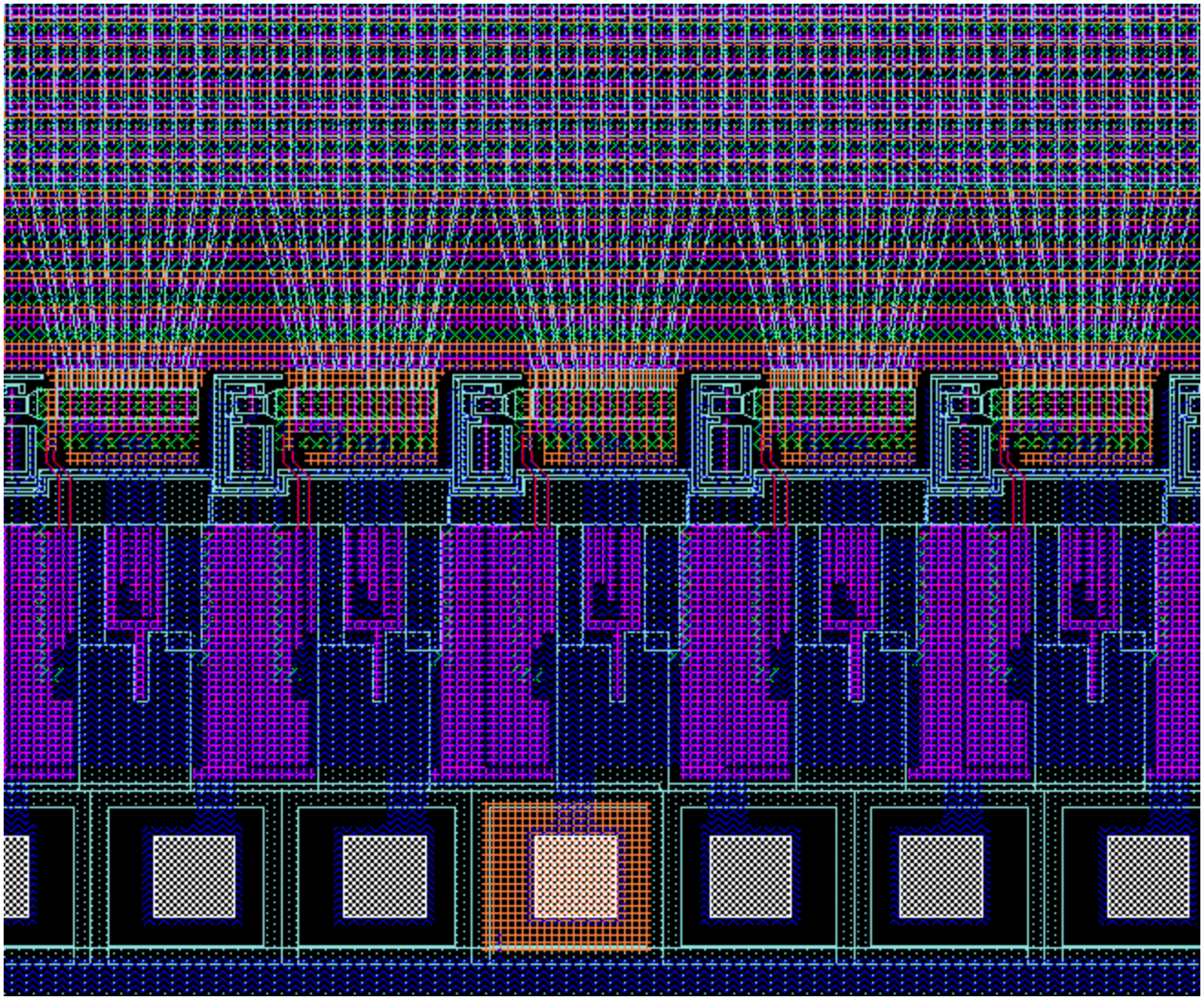
# History of Fast CCD Detector Collaboration



# History of Fast CCD Detector Collaboration

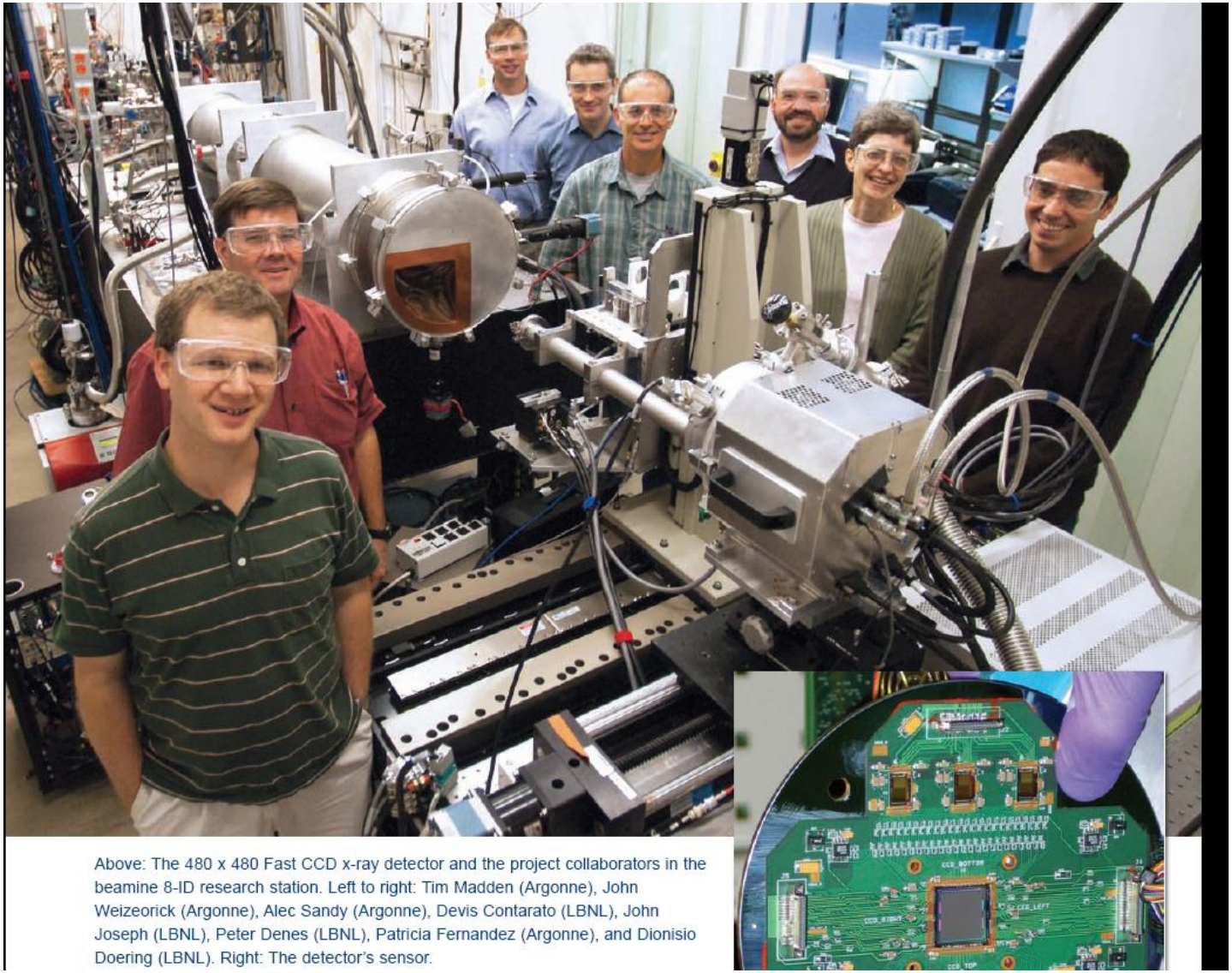
- 480 Fast CCD
  - 480 x 480 (30um pixels)
  - Thick and back-illuminated CCD
    - Good quantum efficiency (QE) for phosphor coupled x-ray cameras
  - Thickness of 200-300 um (Fully Depleted)
    - X-Ray Direct detection
  - Added Almost Column-Parallel Readout
    - Split Top and Bottom of CCD and have one output for 10 columns
  - Targeted Readout time of 2.4 msec readout. Achieved ~6 msec readout
  - 192 Mbytes/sec of raw data
- fCRIC was designed as Custom Readout IC to perform ADC on 96 analog outputs
  - 16 Analog Inputs – 14bit outputs
  - Conversion Rate of 1usec/pixel (Achieved 1.6usec/pixel)
  - 4 Serial LVDS output
- Both CCD and Readout IC are based on SNAP design

# History of Fast CCD Detector Collaboration



P. Denes

# History of Fast CCD Detector Collaboration



Above: The 480 x 480 Fast CCD x-ray detector and the project collaborators in the beamine 8-ID research station. Left to right: Tim Madden (Argonne), John Weizeorick (Argonne), Alec Sandy (Argonne), Devis Contarato (LBNL), John Joseph (LBNL), Peter Denes (LBNL), Patricia Fernandez (Argonne), and Dionisio Doering (LBNL). Right: The detector's sensor.

Not shown: Patrick McVittie, Nord Andresen and Brad Bingham at LBNL; Suresh Narayanan, David Kline, Jonathan Baldwin, and Chris Piatak

# History of Fast CCD Detector Collaboration

## Pictures LBL shows when describing trips to Argonne

# History of Fast CCD Detector Collaboration

## Pictures from my trips to LBNL

Fast CCD X-ray Detector Collaboration between APS and LBNL

# History of Fast CCD Detector Collaboration

## Pictures from my trips to LBNL

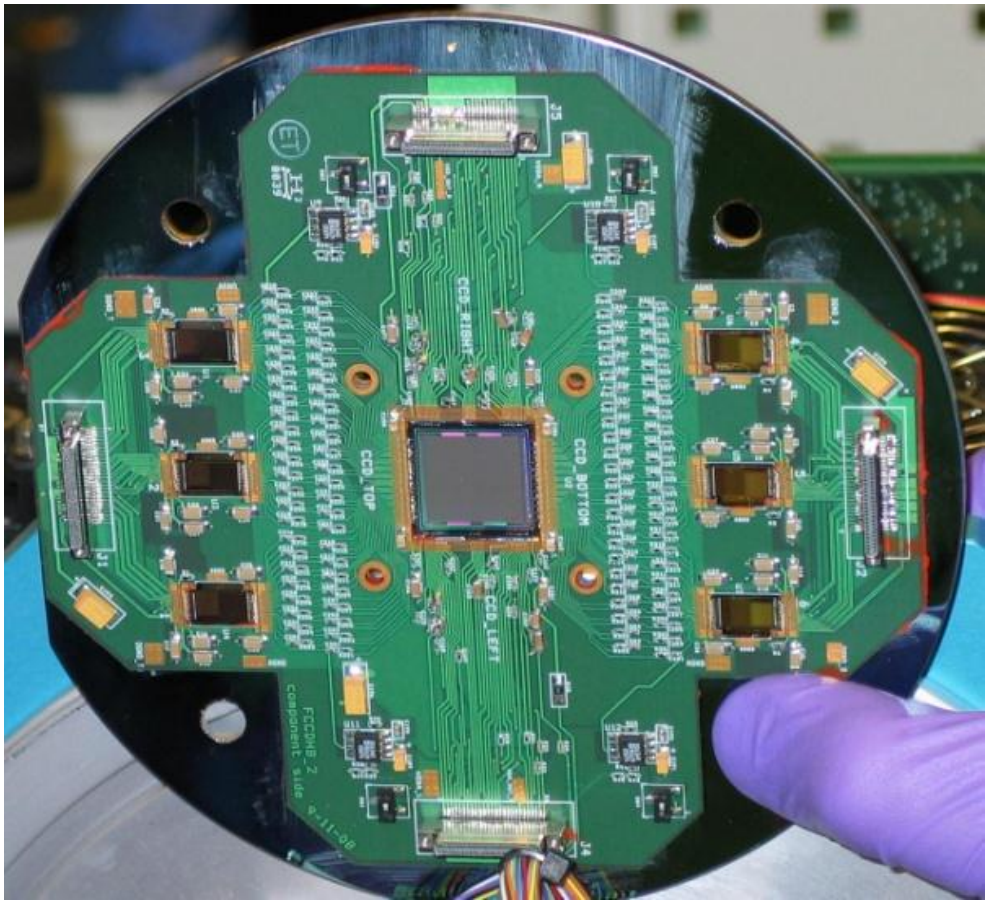
# History of Fast CCD Detector Collaboration

## Pictures from my trips to LBNL

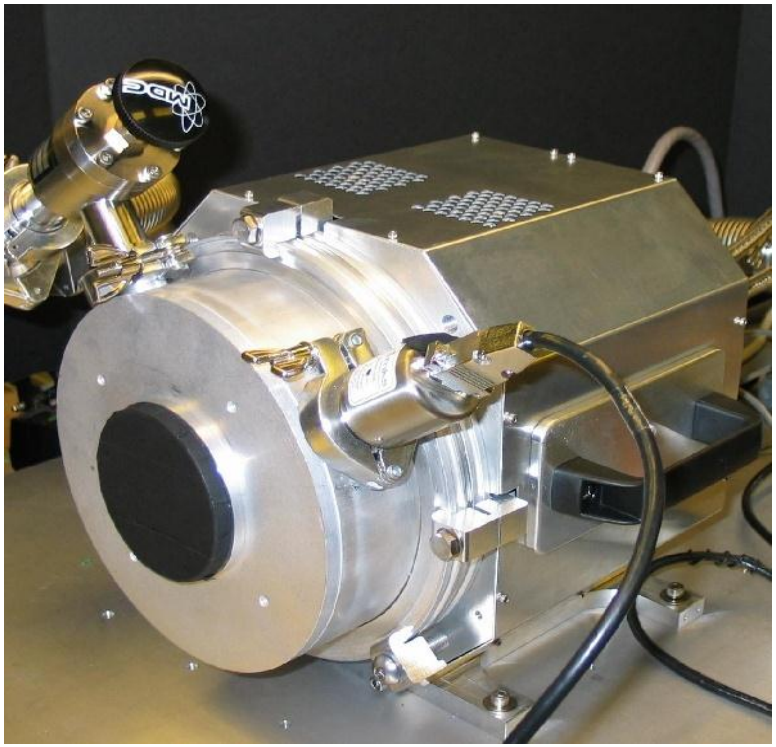
# Summary of Fast CCD Detector Specifications

| Feature | 480 Fast CCD | 2K x 1K Fast CCD | 2K x 1K Fully Parallel FCCD |
|---|---|---|---|
| Area | 480 x 480 | 1920 x 960<br>960 x 960 frame transfer mode | 1920 x 960<br>960 x 960 frame transfer mode |
| Thickness | 250 µm | 250 µm – 350 µm | 250 µm – 350 µm |
| Pixel Size | 30 $\mu m^2$ | 30 $\mu m^2$ | 30 $\mu m^2$ |
| QE | Near 1 at 8keV | Near 1 at 8keV | Near 1 at 8keV |
| Readout Speed | 36 MegaPixes/sec<br>- 125 fps (no exps time) | 200 MegaPixels/sec<br>- 220 fps frame store mode | 1000 to 10,000 MegaPixels/sec |
| Full Well | ~900k $e^-$ per pixel<br>~150000$e^-$ in 8x Mode | ~900k $e^-$ per pixel | ~900k $e^-$ per pixel |
| Gain | 6$e^-$/ ADU for 8x<br>23.7 eV/ADU for 2x | 6$e^-$/ ADU for 8x<br>23.7 eV/ADU for 2x | TBD |
| ADC precision | 13 bits,<br>2 extra bits for gain | 13 bits, Improved Linearity!<br>2 extra bits for gain | 10 bits,<br>2 extra bits for gain |
| ADC speed | 625 KHz | 1 – 2 MHz | 80 MHz |
| Unique Features | Thick, fully depleted, Back Illuminated, **almost column-parallel readout** which allows a fast readout with low noise | Frame Transfer Mode, Larger than 480 FCCD, Thick, fully depleted, Back Illuminated, **almost column-parallel readout** | Frame Transfer Mode, Thick, fully depleted, Back Illuminated, **column-parallel readout** |
| Available | 1 ½ detector available | Two at APS in June 2012 | 3 to 5 years of development |

# 1st Generation Detector - 480 Fast CCD Detector At APS

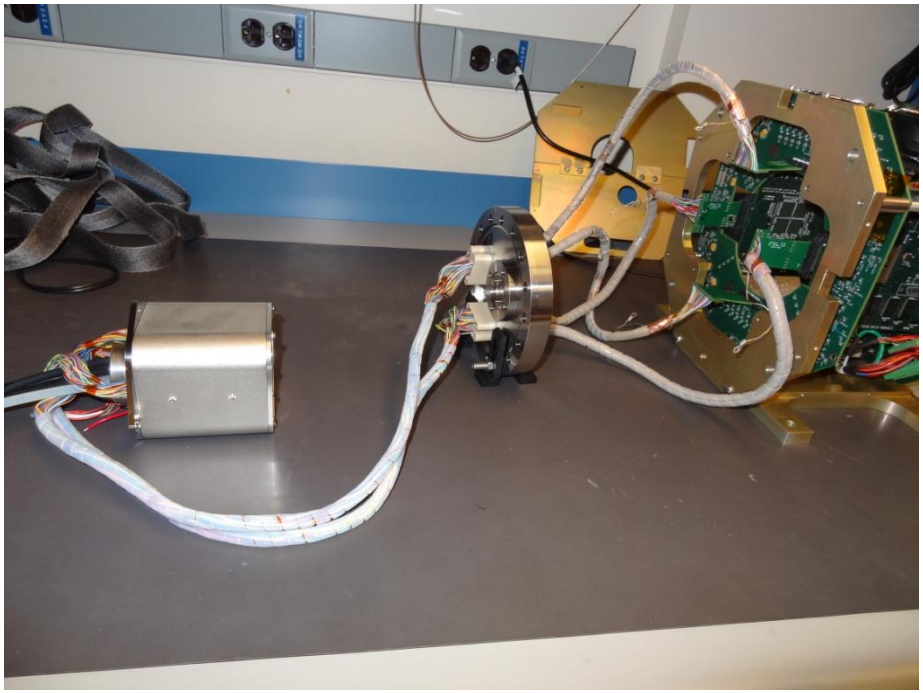


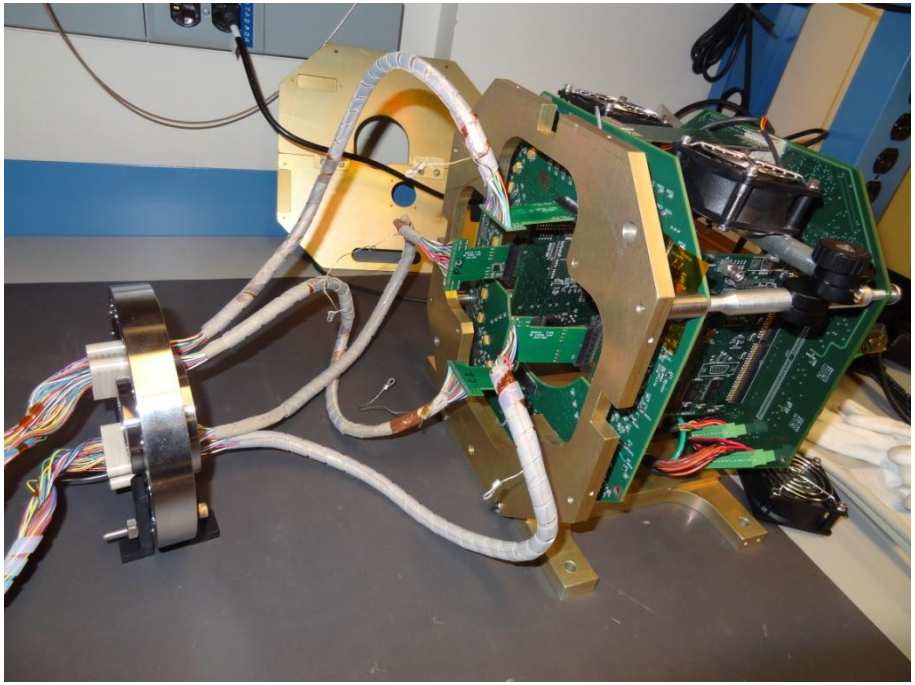
Sensor Assembly for APS 480 FCCD

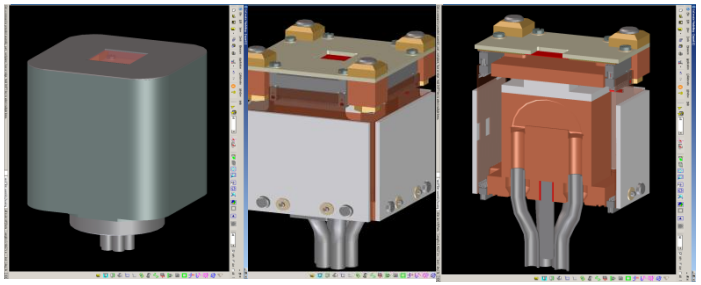


# 1st Generation Detector - 480 Fast CCD Detector At ALS

LBNL 480 Fast CCD with Compact Head
Used at ALS and LCLS
Going Inside Nanosurveyor at ALS ~ 2012







# 2nd Generation Detector – 1K Frame Store CCD

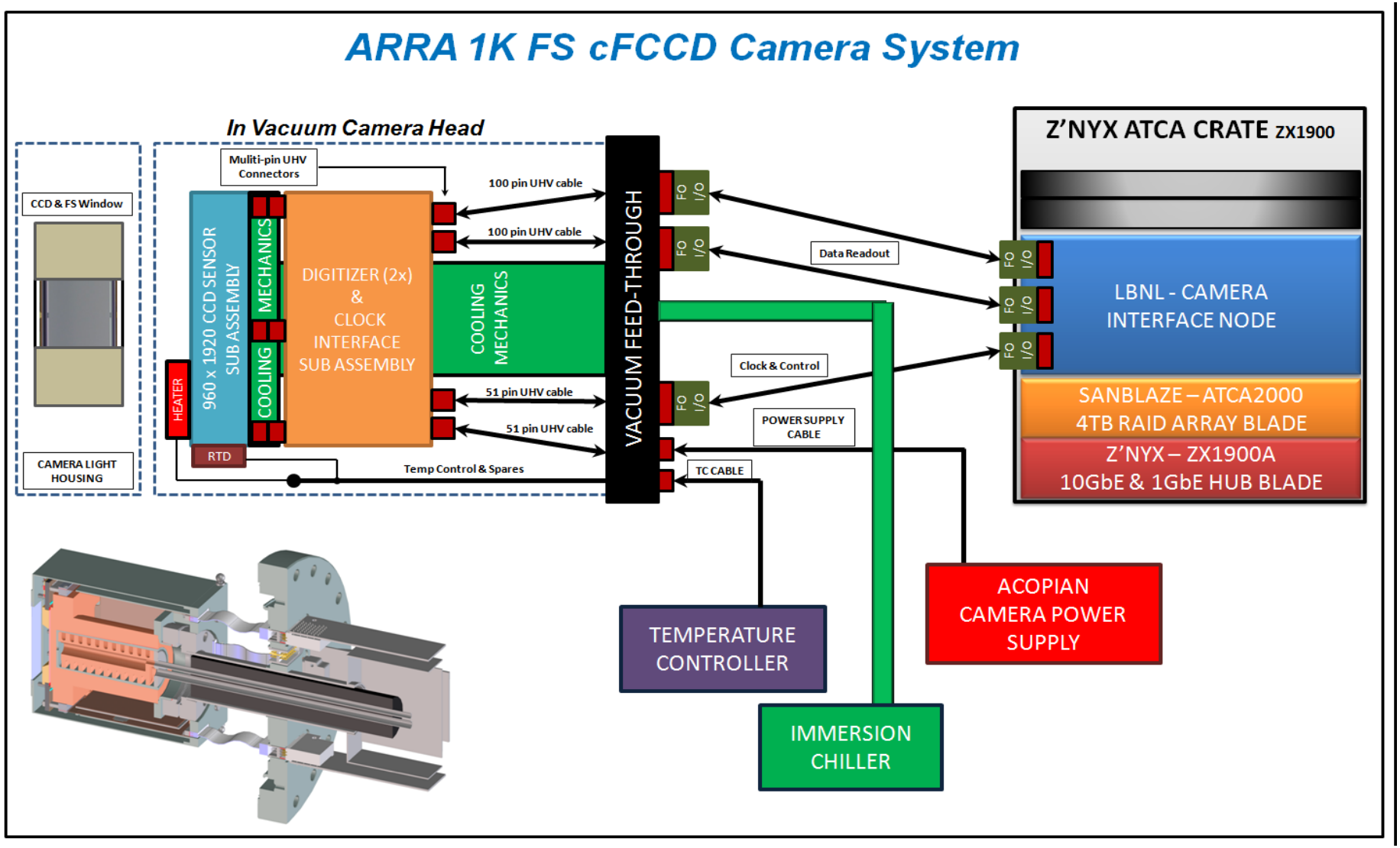
Initiation of Project

- LBNL started design work on 1KFSCCD with internal funding
  - New CCD Design and fCRIC2 design
- Both ANL and LBNL Received ARRA Funding in July 2009
  - APS to build two 1KFSCCDs and LBNL to build eight 1KFSCCDs

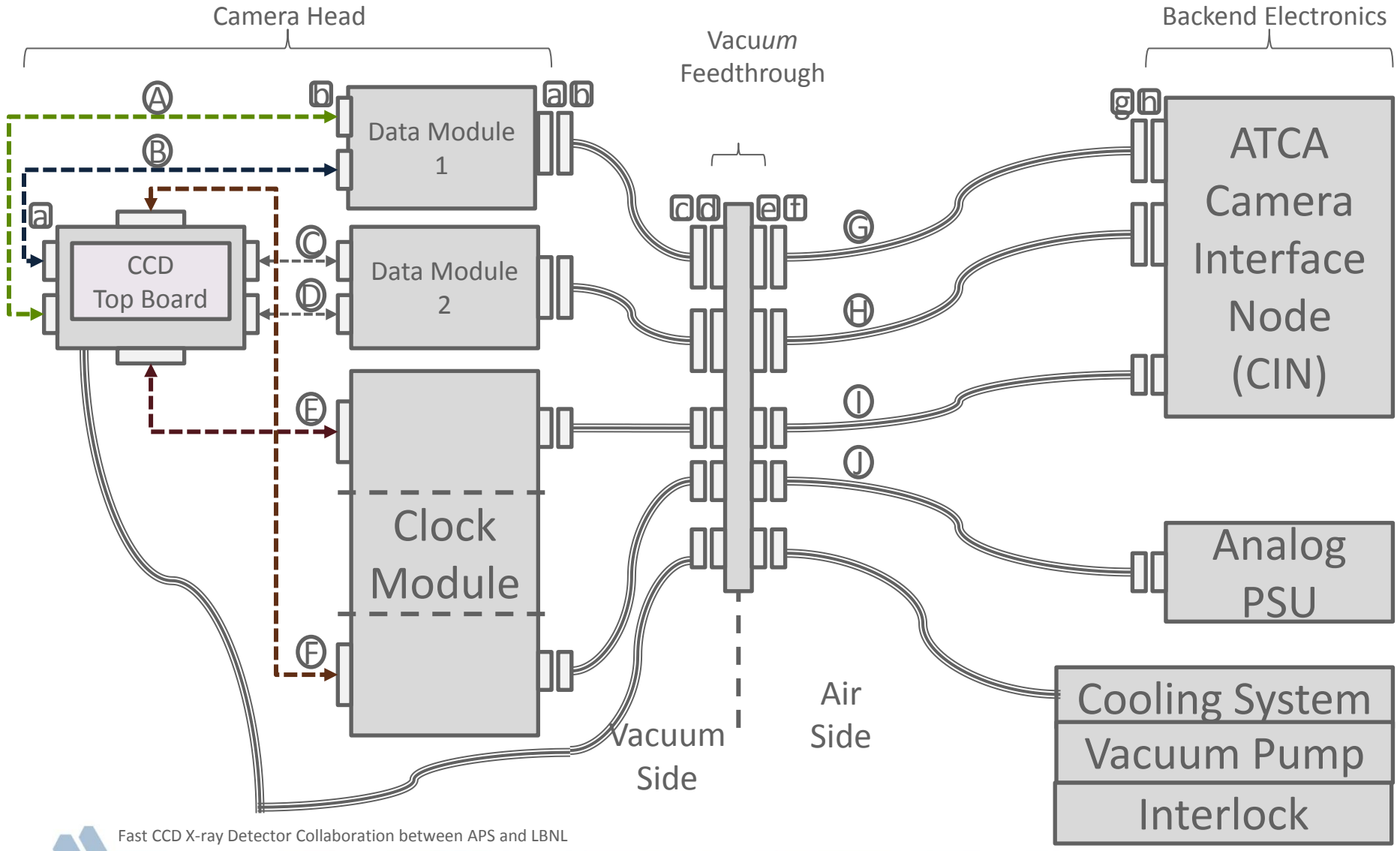
1K Frame Store CCD Characteristics

- Based on 480 FCCD Detector (with improvements)
- CCDs still use 10 Columns per Analog output
- 1920 x 960 CCD with a 960 x 960 Frame Store Mode
- Develop fCRIC2 readout chip
  - Fix non-linearity and add more power supply rejection
  - Fix speed limitation – Tested at 1µs. Plan to run at .8µs (old fCRIC = 1.6µs)
- Add Buffer chips on Analog Outputs
  - Improve readout speed
  - Improve signal to noise

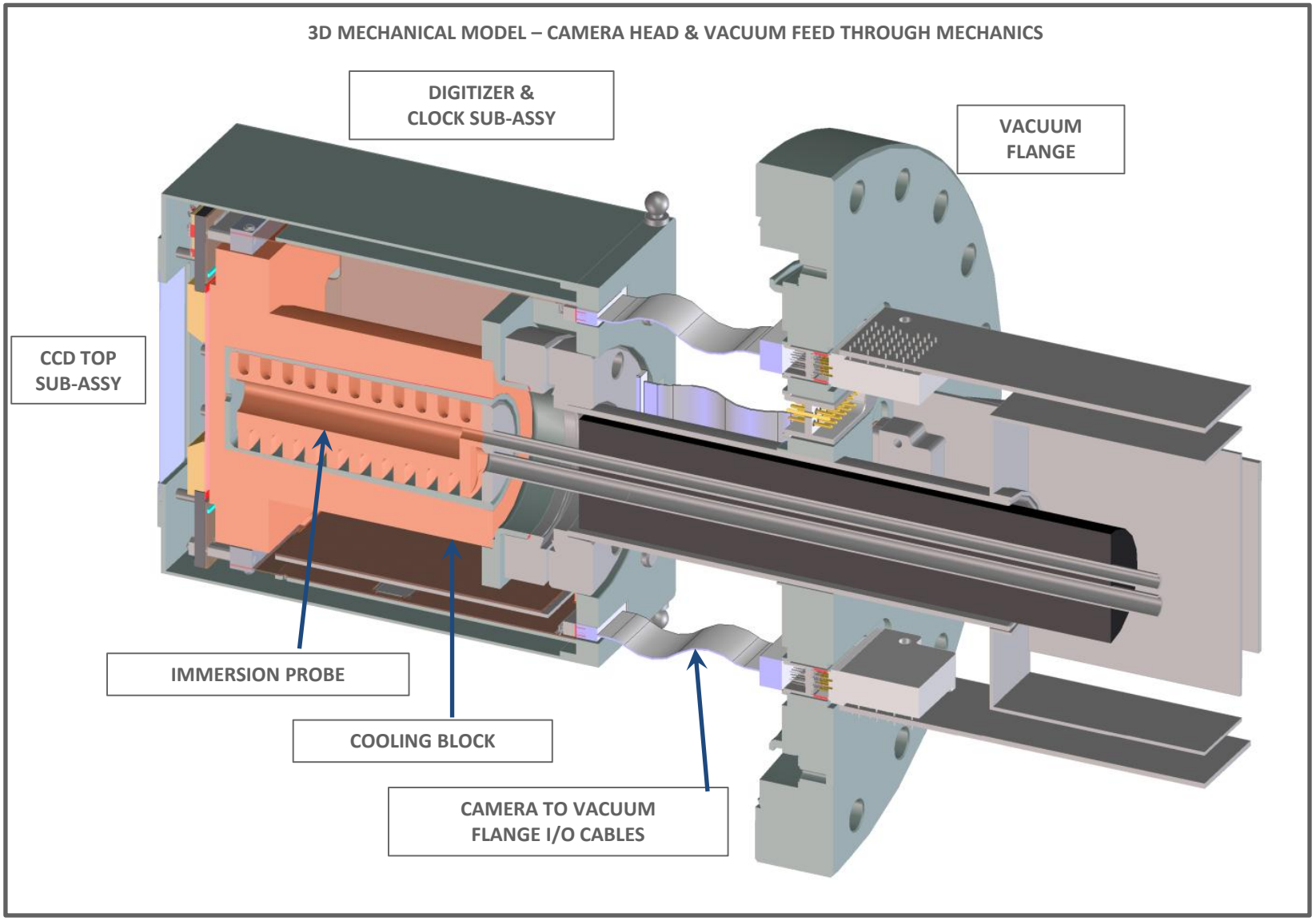
# 1kFSCCD – System Block Diagram



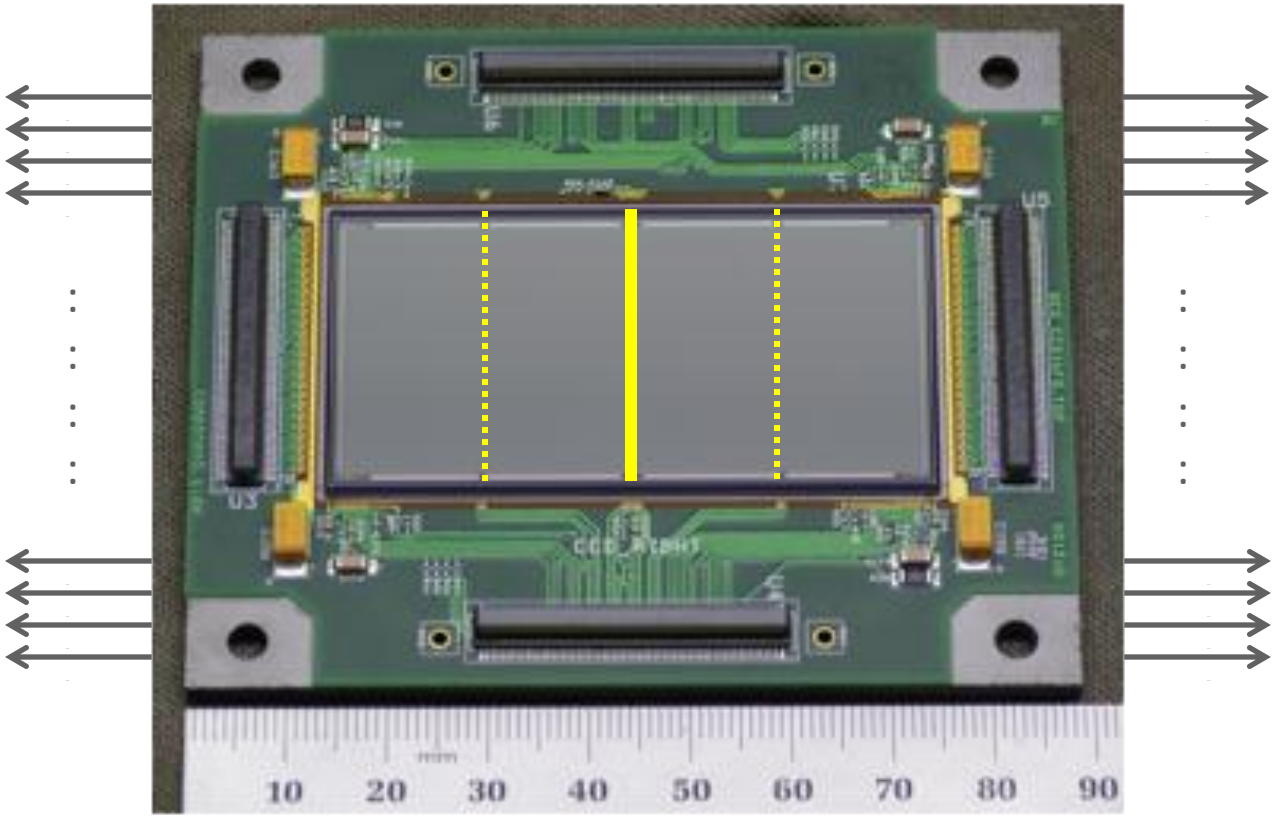
# 1kFSCCD - Block Diagram



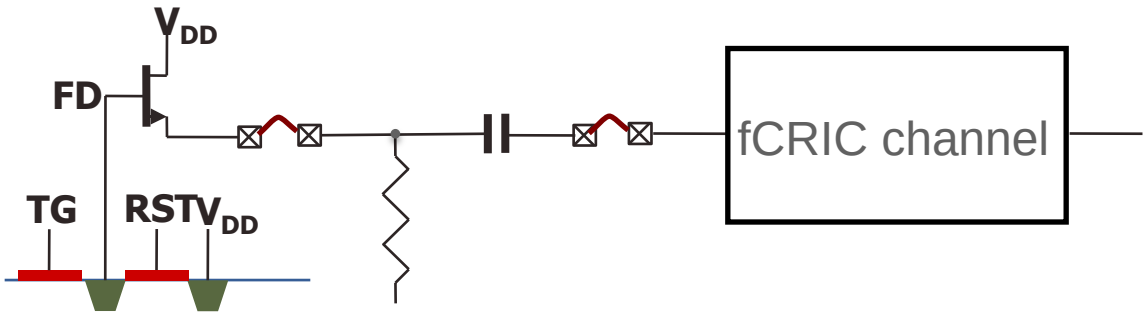
# 1kFSCCD – Detector Head Cutaway



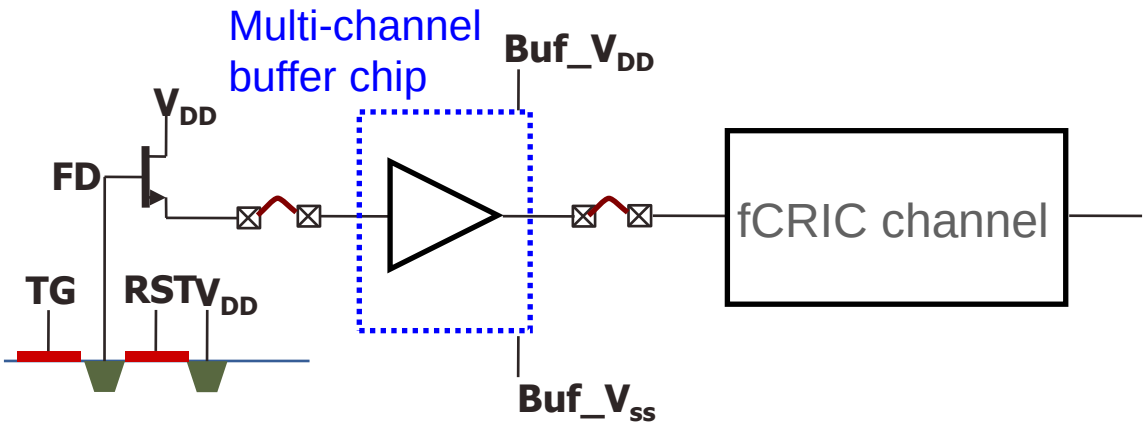
# 1kFSCCD – Top Board with CCD



# 1kFSCCD – Top Board Buffer Chip



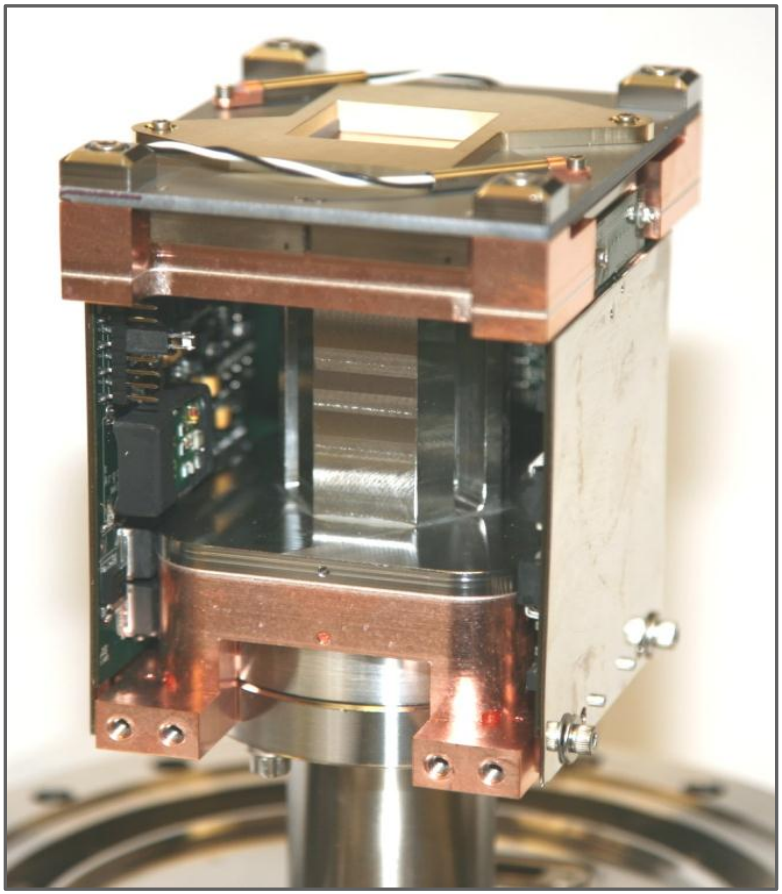

- ☹ Output SF $g_m$
- ☹ SF drives large load cap
- ☹ Resistive bias
- ☹ AC-coupling

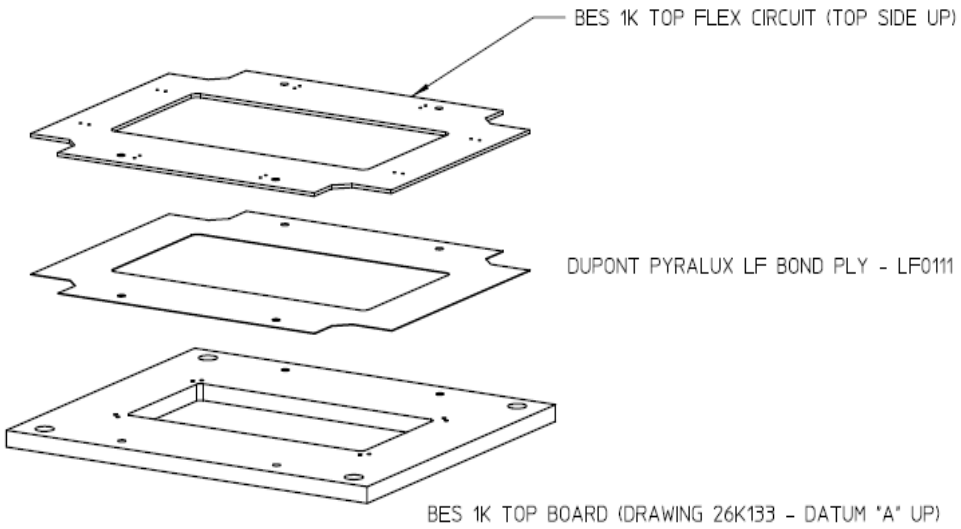



- ☺ SF drives small load cap
- ☺ Current source bias
- ☺ DC-coupling

- Simply waiting for PCBs (and assembly) – delayed (problems at PCB house)
  - Results soon – (Tested on 480 version but smoked first 1KFSCCD assembly in March 2012)

# 1kFSCCD – Top Board Stack up

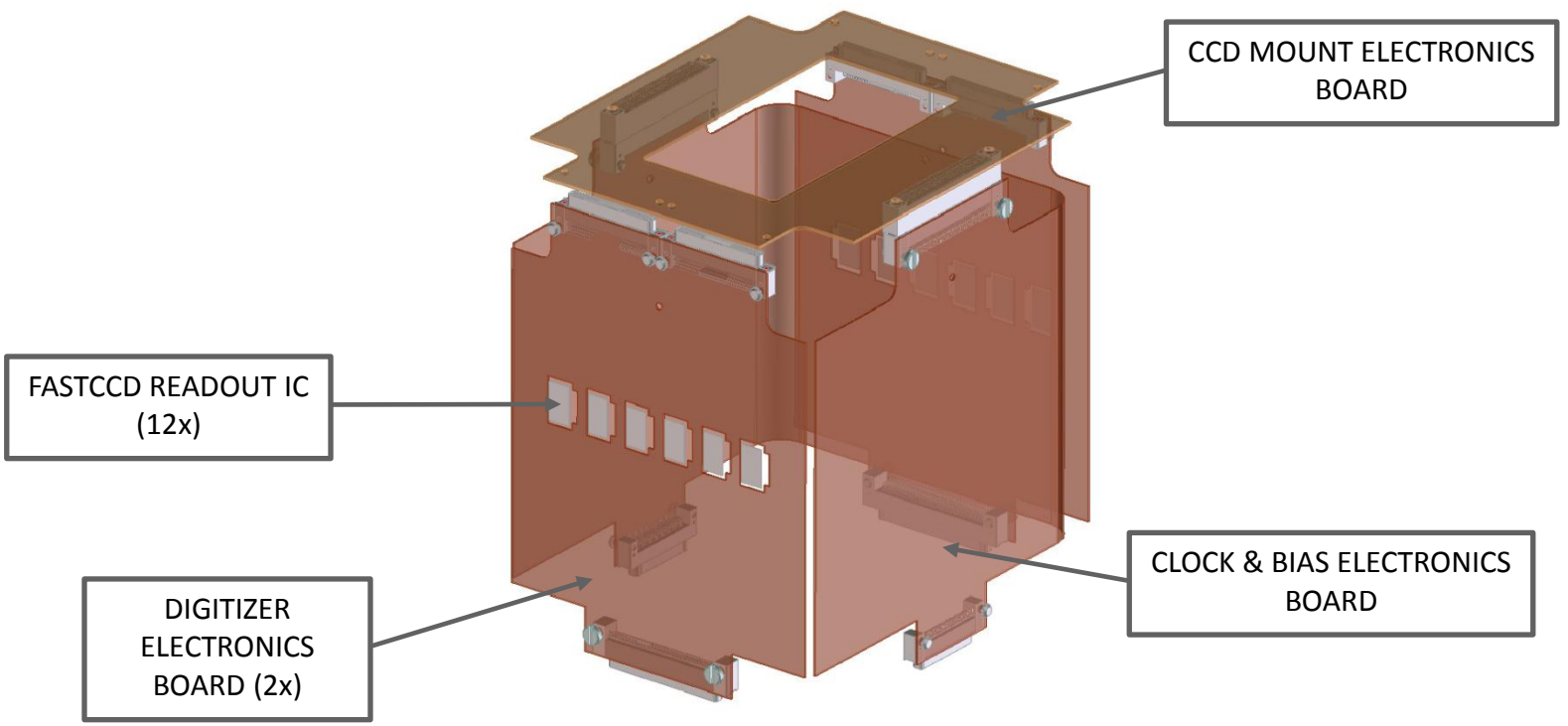




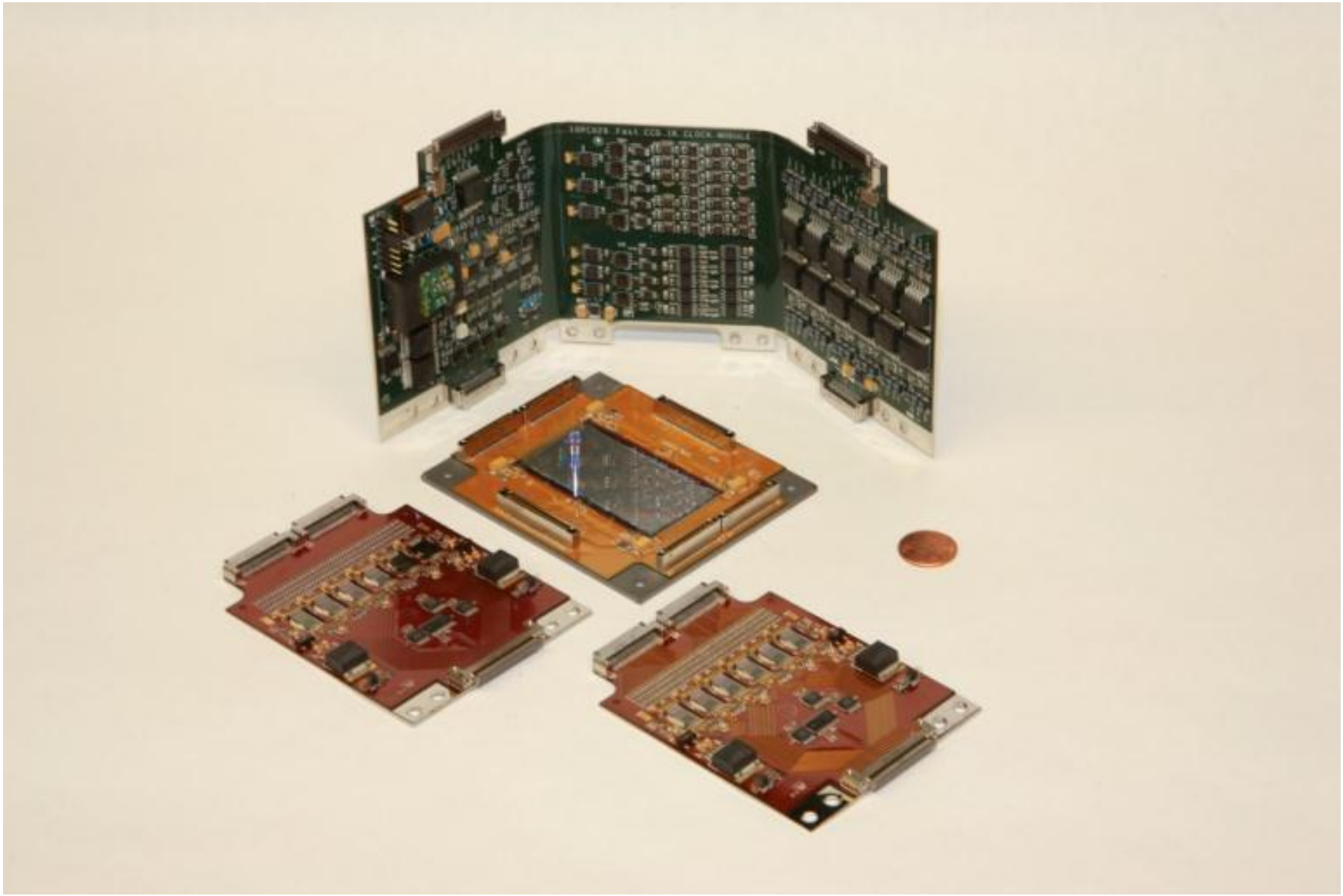

Silicon Nitride plate used for Cooling

- Good thermal conductor
- Coefficient of expansion similar to Silicon
- $Si_3N_4$ Linear coefficient of Expansion 3.3 x $10^{-6}$ /˚C
- Si Linear Coefficient of Expansion 3 x $10^{-6}$ /˚C

# 1kFSCCD – Detector Head

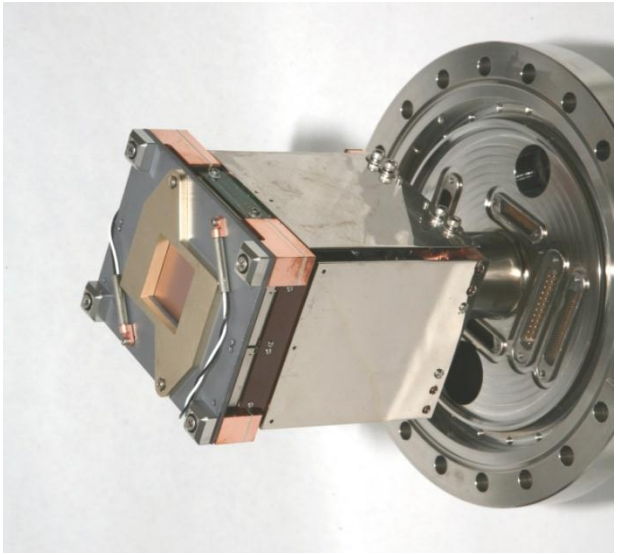


# 1kFSCCD – Detector Head

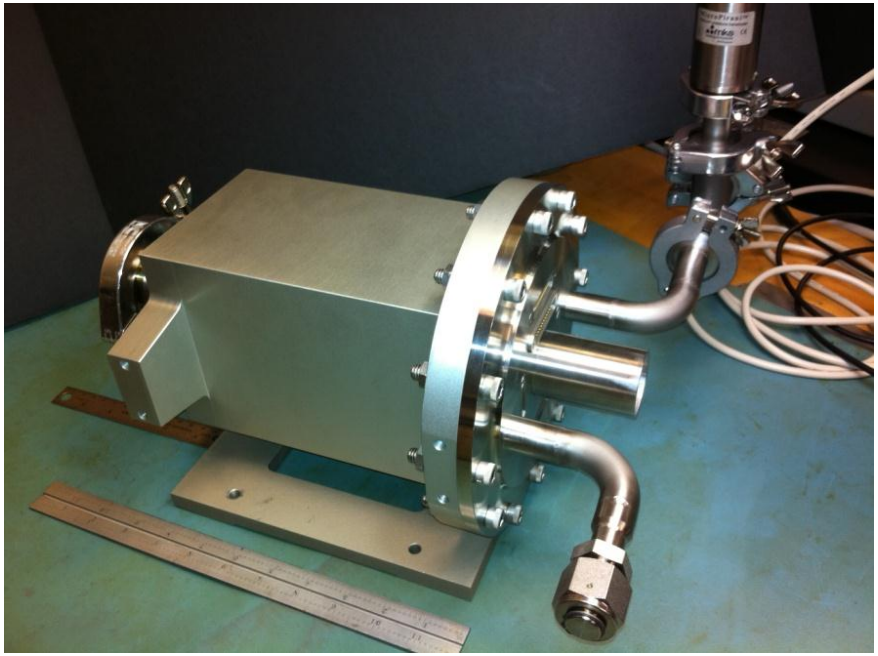


# 1kFSCCD – Vacuum Chamber

LBNL Vacuum Chamber



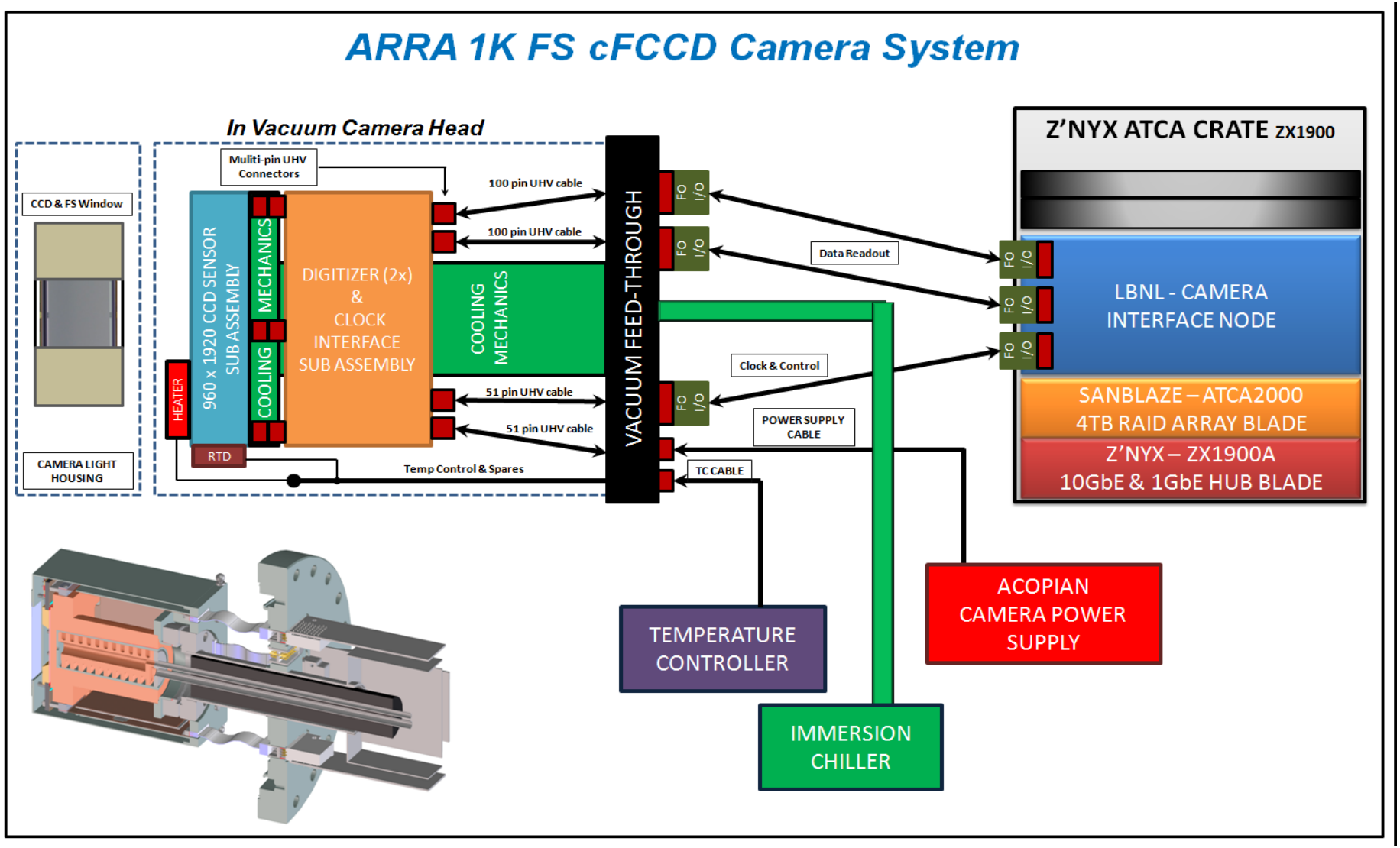
APS Vacuum Chamber



Characteristics shared by both vacuum chambers

- Main 8 inch Vacuum flange
- Connectors and their locations
- Center Tube and Conflat flange used to mount the detector head

# 1kFSCCD – System Block Diagram



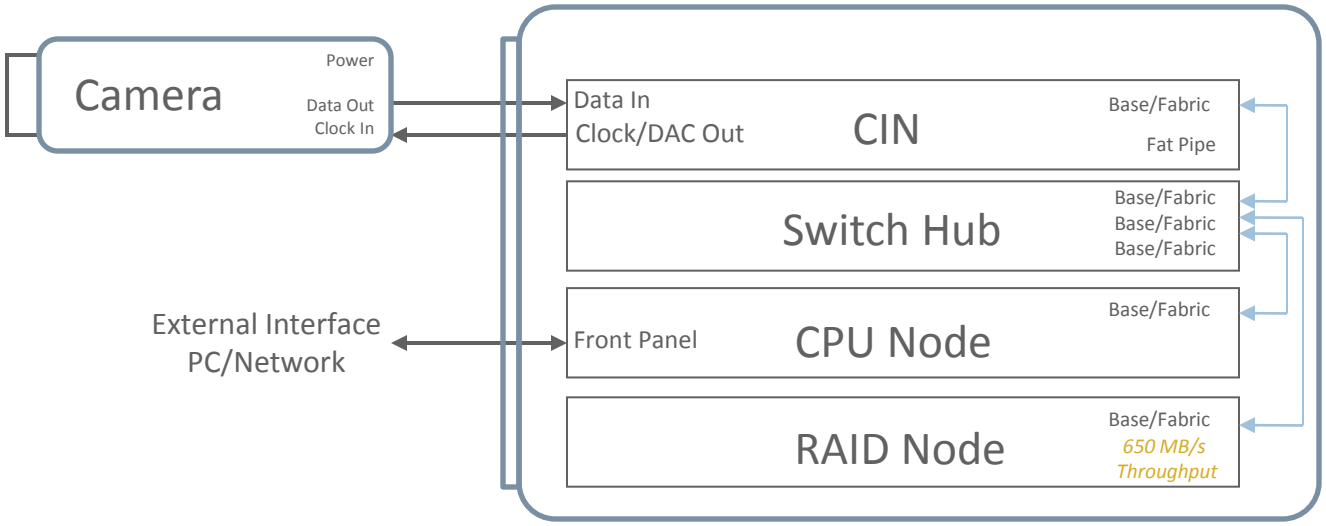
# 1kFSCCD – Data Flow Requirements

| Parameter | System Requirements | System Benchmarks | Theoretical Hardware Limit |
|---|---|---|---|
| Total Pixels | 960 x 960 FS<br>960 x 1920 | NA | NA |
| Frame Rate (Continuous)<br>To RAID | 200 fps | 214 fps | 285 fps |
| Frame Rate (Burst)<br>To CPU DDR | None | 365 fps | 625 fps |
| Time Capacity<br>Data to RAID | 1.0 Hr | 2.0 hrs | 2.1 Hrs |
| Frame Size (Raw) | 2.0 Bytes * (960*960) | NA | NA |
| Network Bandwidth | 370 MB/s | 730.0 MB/s | 1,250.0 MB/s |
| RAID Write Speed | 370 MB/s | 396 MB/s | 570.0 MB/s |
| RAID Size | 2,000,000 MB | 2,855,298 MB | 3,000,000 MB |
| Frames Max<br>Stored on RAID | 1,000,000 | 1,427,649 | 1,500,000 |

# 1kFSCCD – ATCA Block Diagram

ATCA System: Minimal signal processing, readout direct to RAID

Throughput Limit == Camera to RAID: 650 MB/s

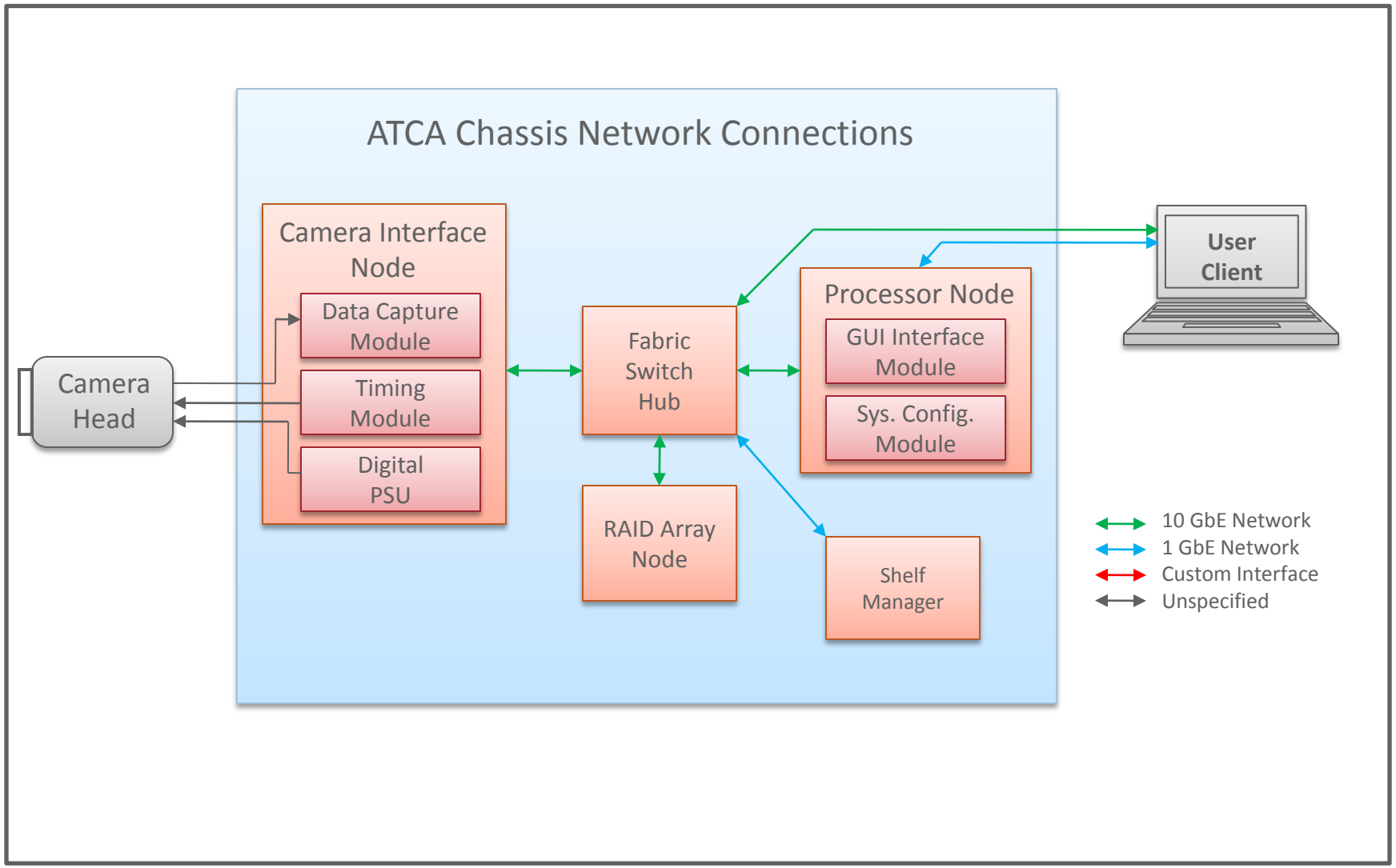



370MB/s >> ($960^2$ pixels x 2 Bytes x 200 fps) >> 1.4TB/hour

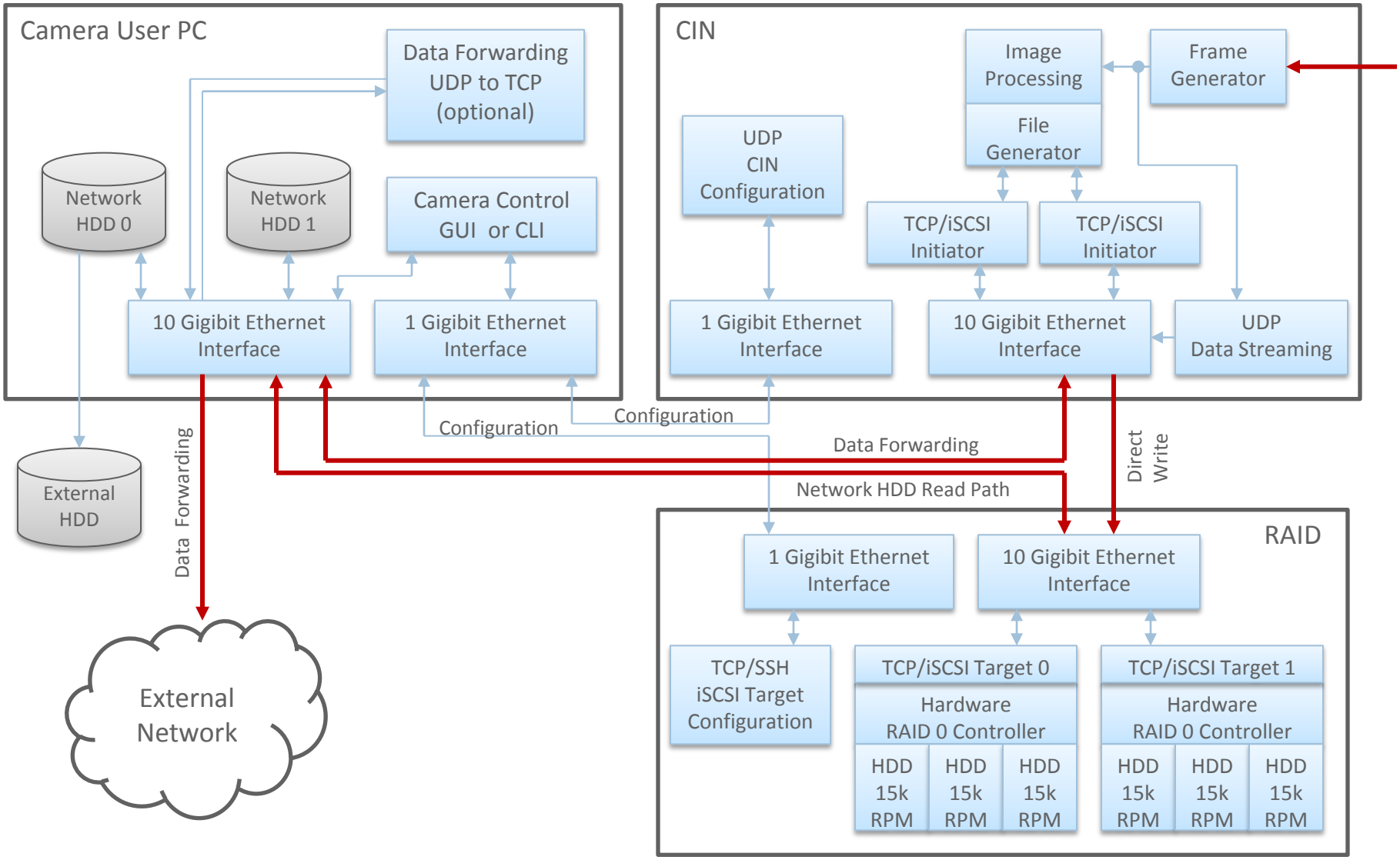
: Custom Inter-board Connector
: 10 GbE Fabric and 1 GbE Base
CIN: Camera Interface Node

# 1kFSCCD – ATCA

# 1KFSCCD Data Flow

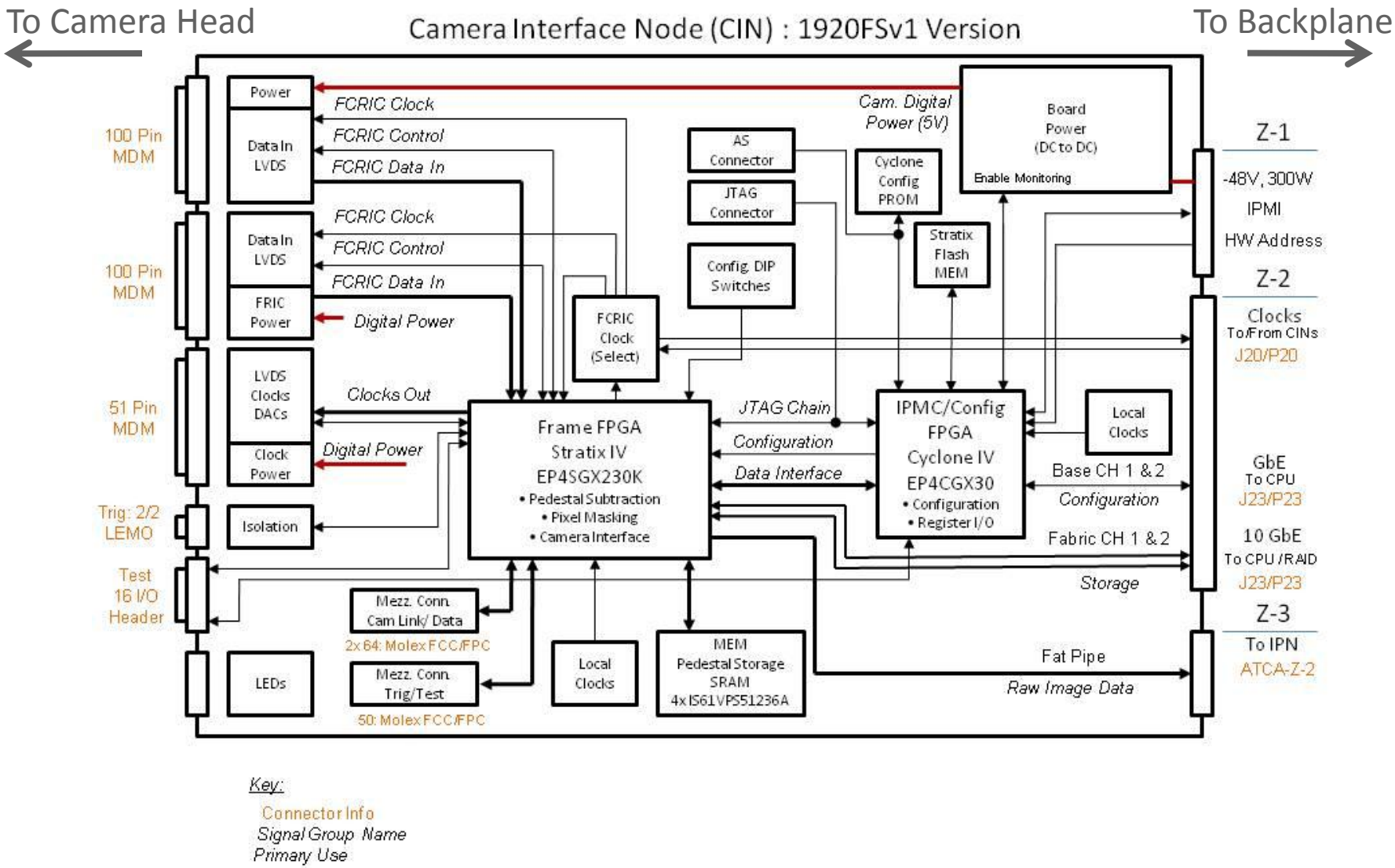


# 1KFSCCD Data Flow

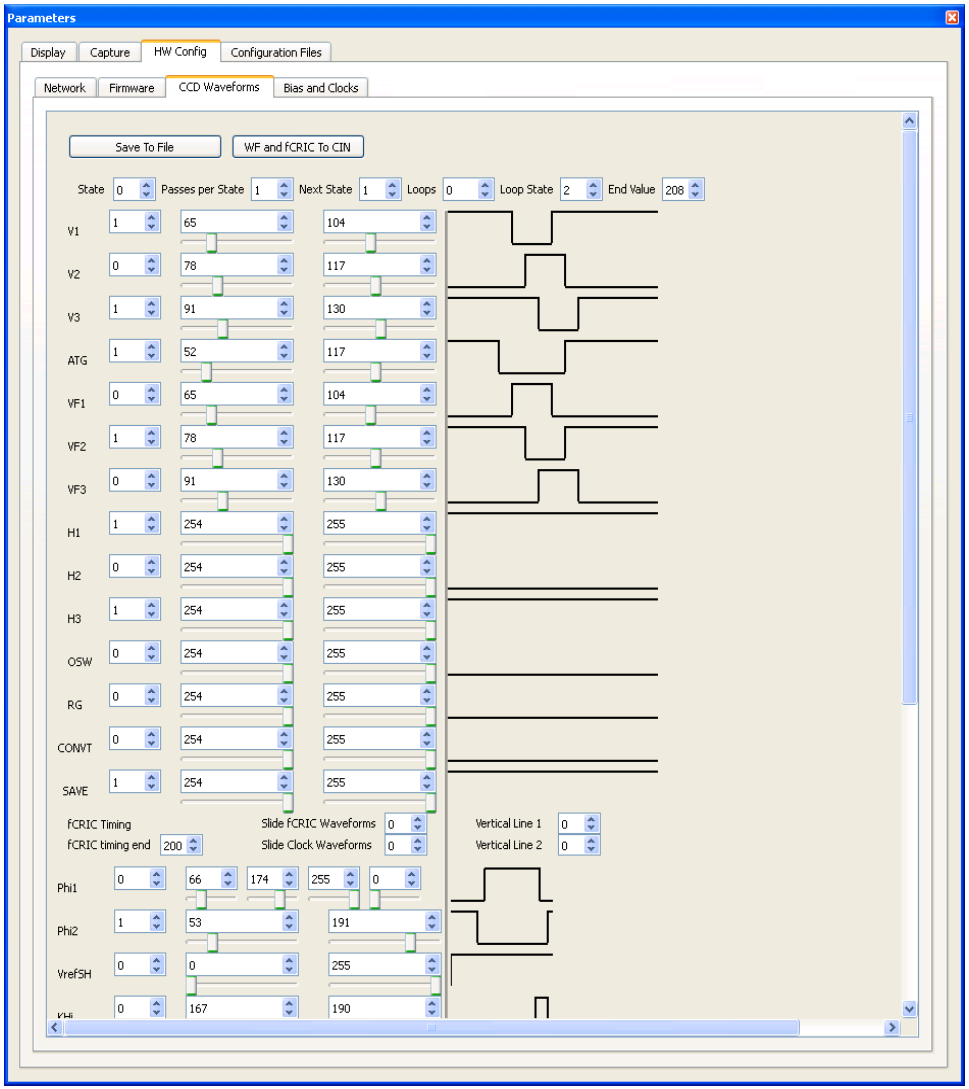


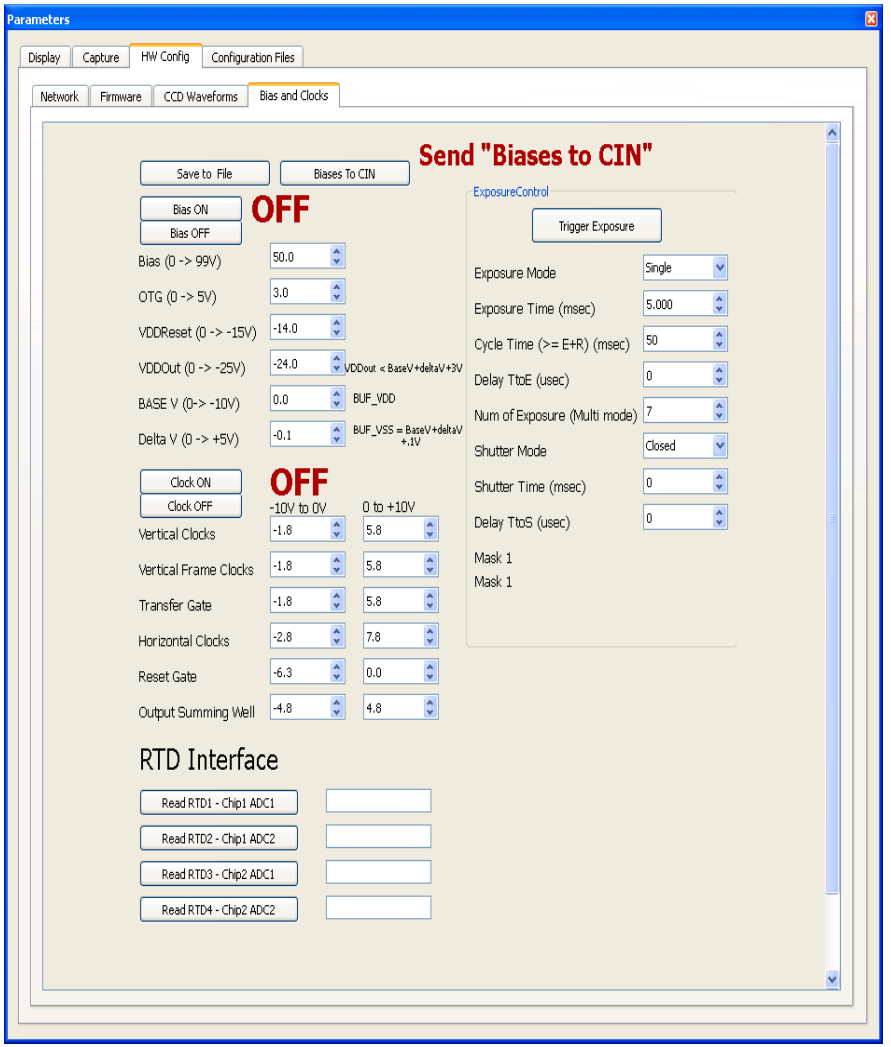
# 1kFSCCD – CIN (Camera Interface Node)

# 1kFSCCD – CIN Block Diagram

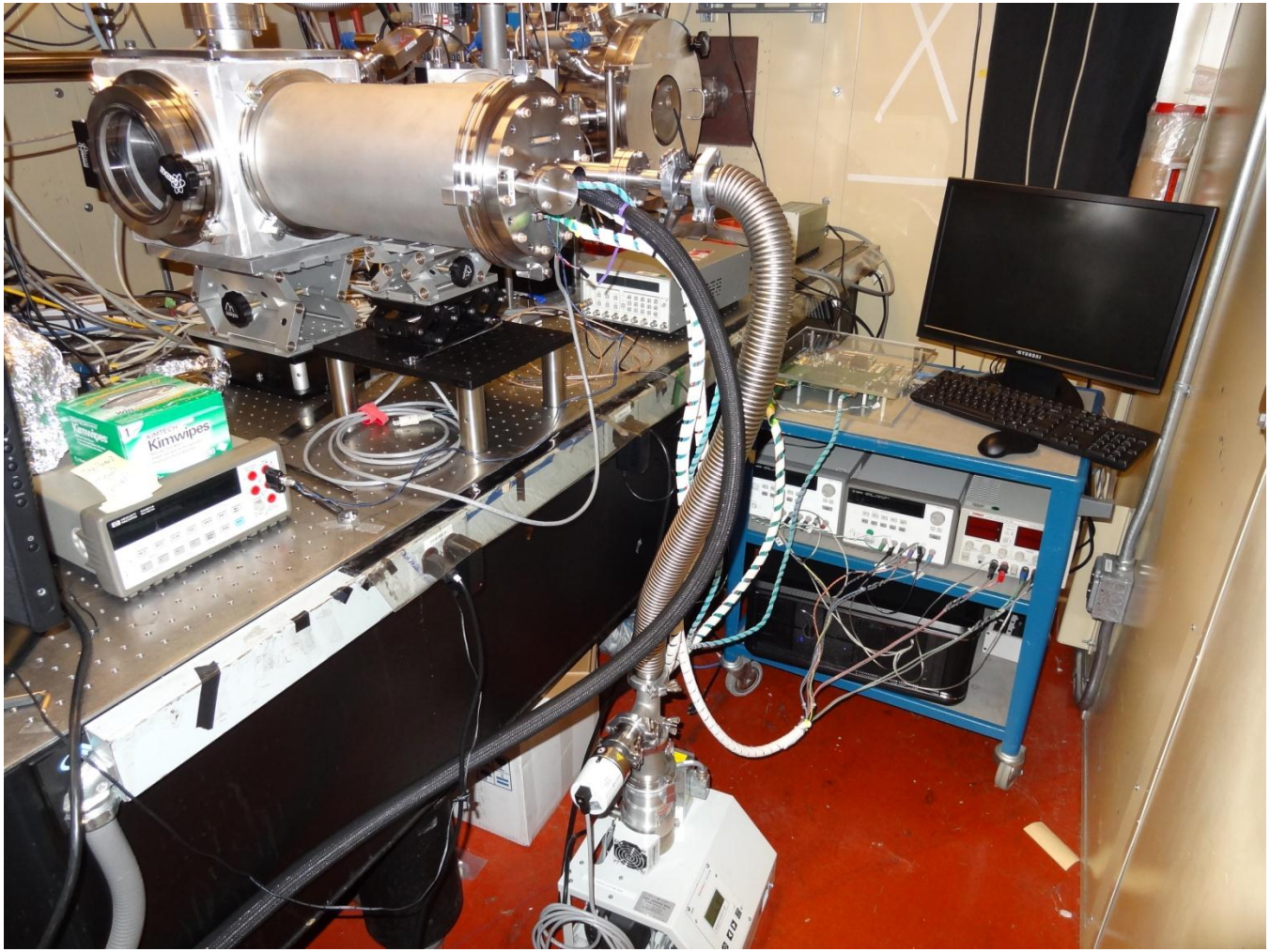


# 1KFSCCD - Development GUI

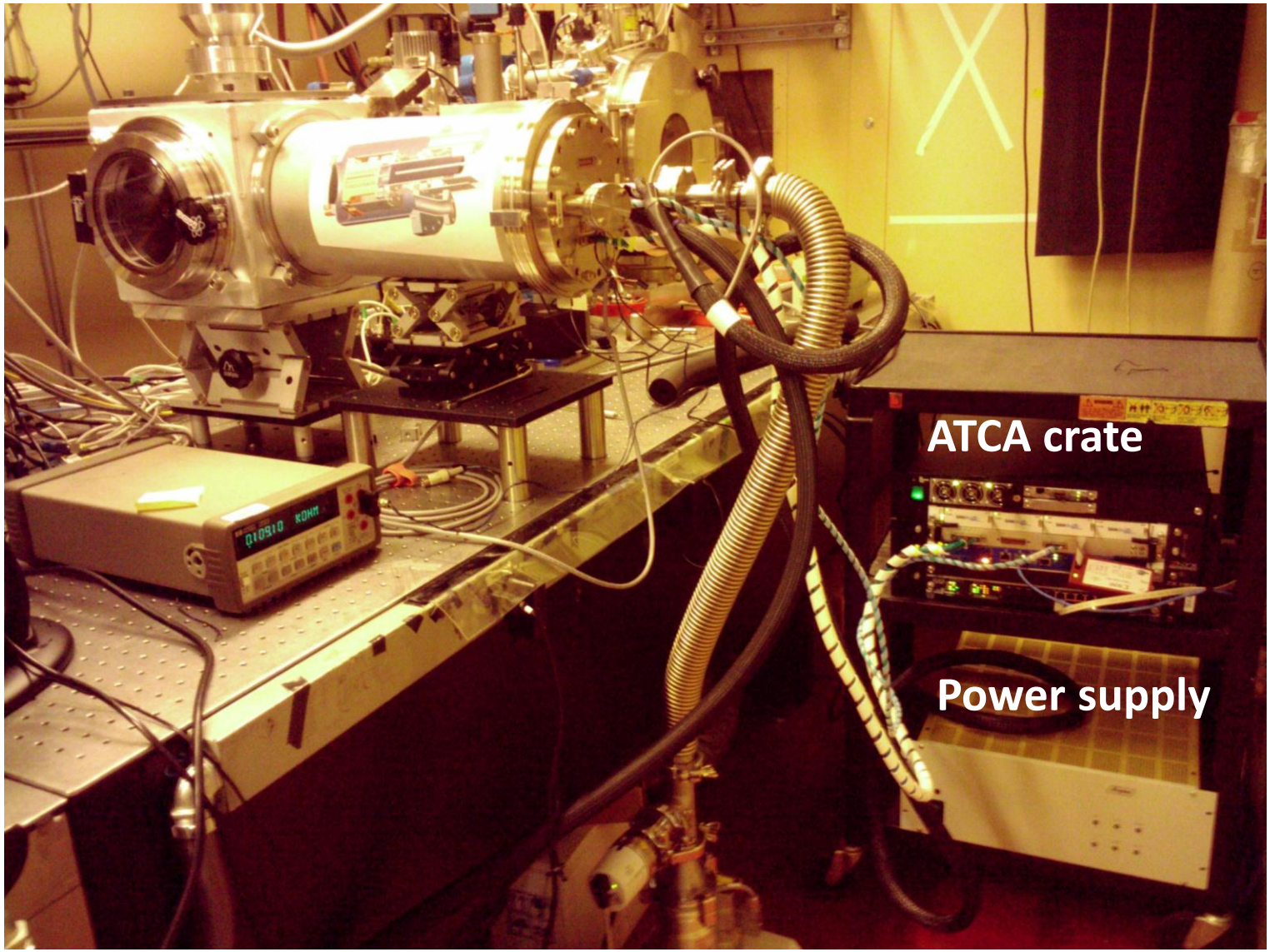


# 1KFSCCD at 3.5.1 Beamline in March

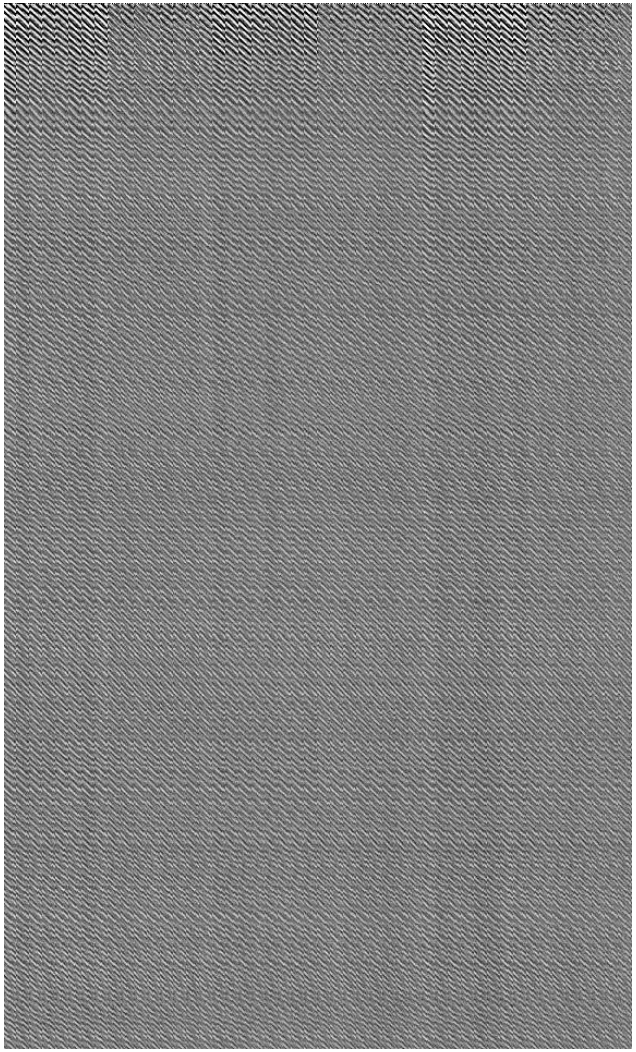


# 1KFSCCD at 3.5.1 Beamline in April

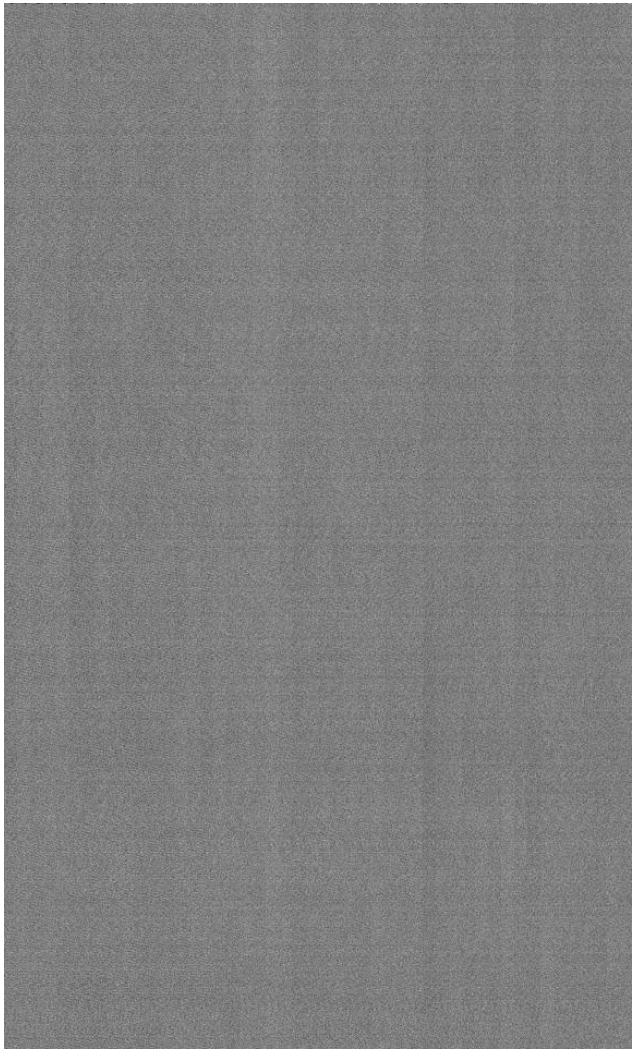


# Sample images (dark subtracted)

Before

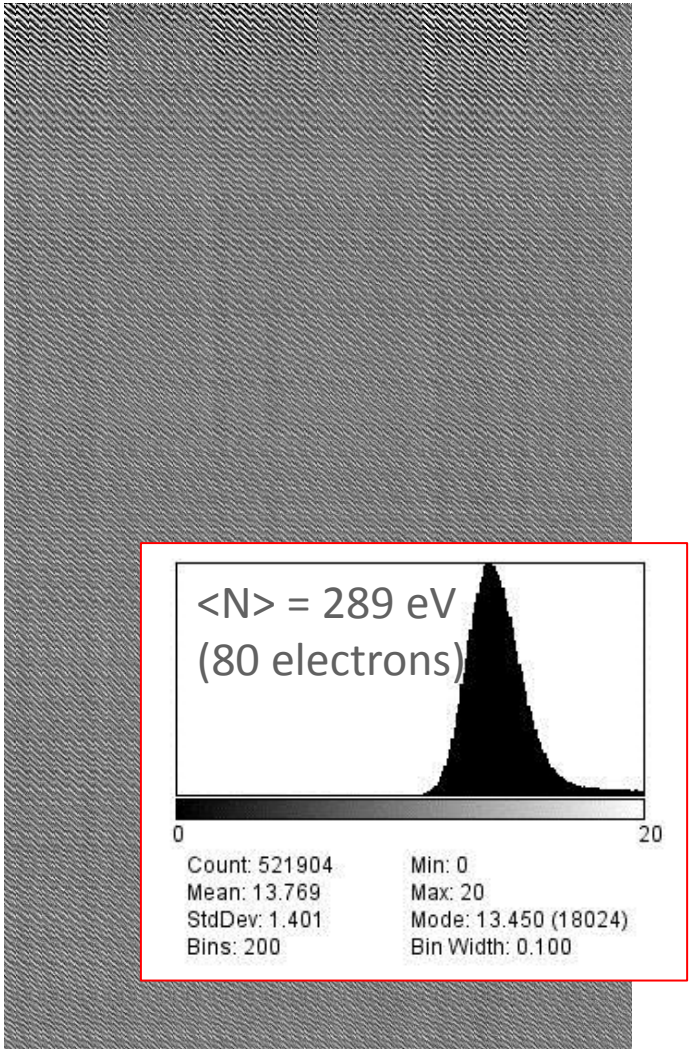


Now

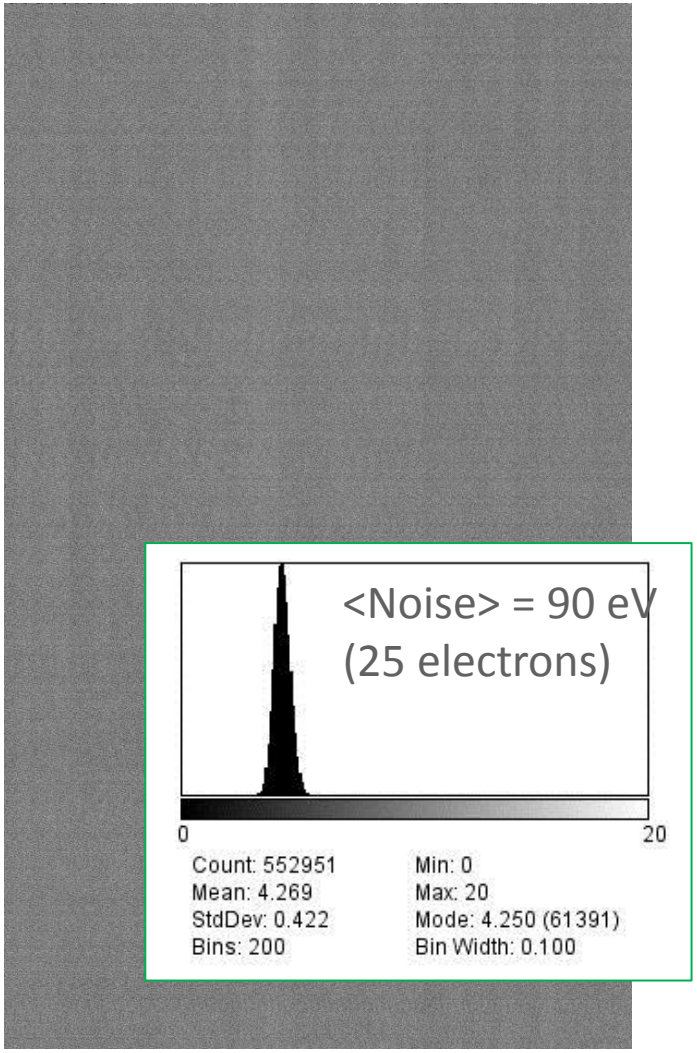


# Noise improvement

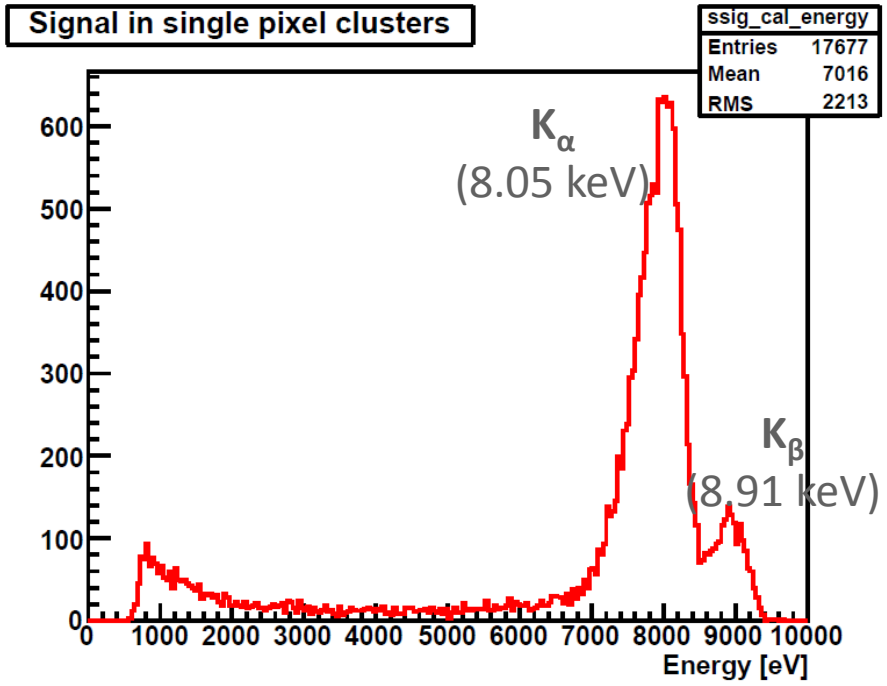
**Before**

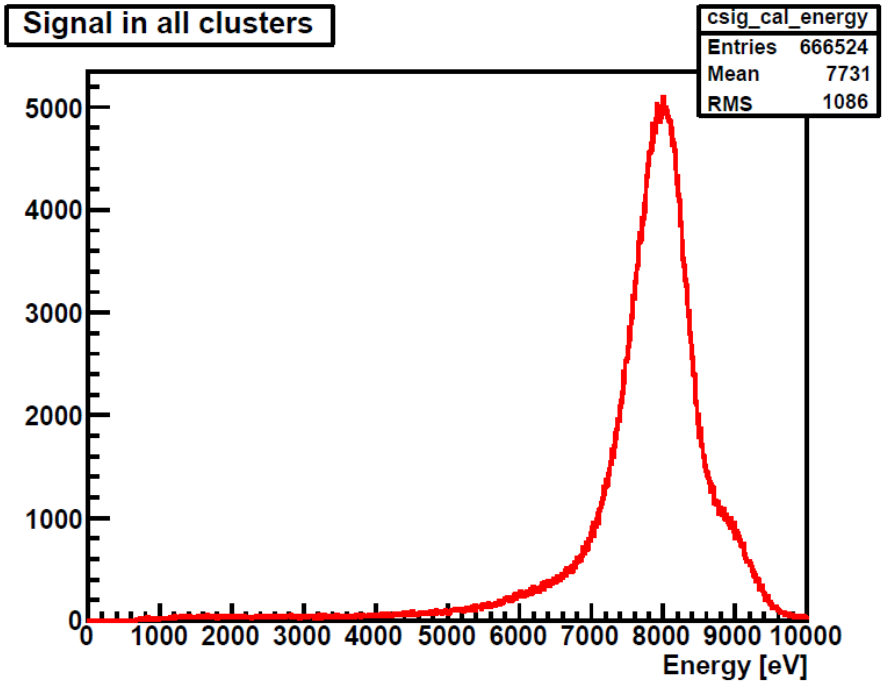



**Now**



# Sample results from Cu fluorescence (preliminary)




- T = -50°C, exposure time = 20 ms, $V_{dep}$ = 50 V
- Calibration algorithm still under development

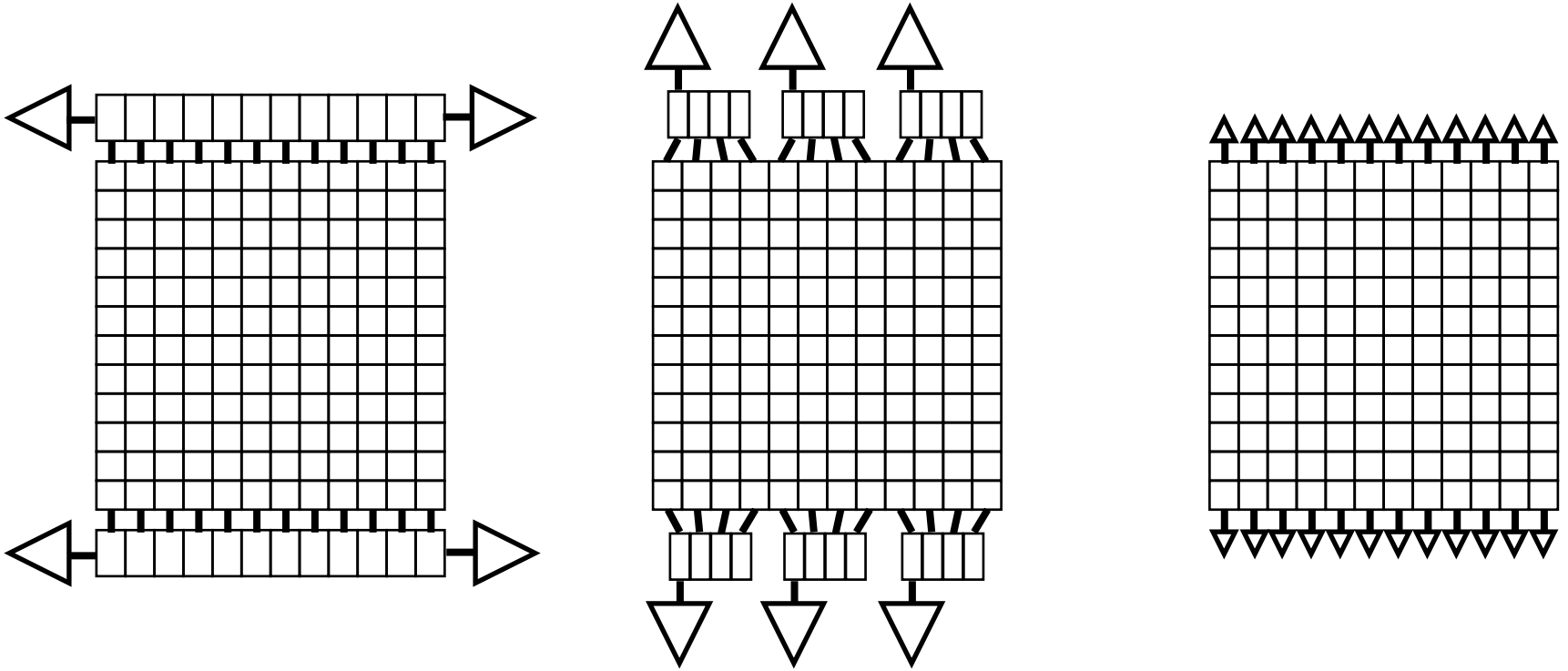
# 2nd Generation Detector – 1kFSCCD Time Line

| Date | Mile Stone |
|---|---|
| July 2009 | ARRA Funding |
| September 2010 | Design Review at LBNL |
| December 2010 | Specified Acopian Power Supply Design |
| February, 2011 | Received First 2 Clock Module |
| April 2011 | Received 3 Acopian Power Supplies |
| July 2011 | Ordered two 6 Slot ATCA Shelves |
| October, 2011 | Received Flange for Vacuum Chamber 1 from SRI |
| March 2012 | Received Flange for Vacuum Chamber 2 from SRI |
| March 2012 | Received two 6 Slot ATCA Shelves |
| April 2, 2012 | Start production of Clock Modules |
| April 3, 2012 | LBNL takes data at 5.3.2 with 1st 1KFSCCD Back Processed Using ATCA Crate and Acopian Power Supply |
| June 29, 2012 | End of ARRA Project |

# 3rd Generation Detector – Very Fast CCD

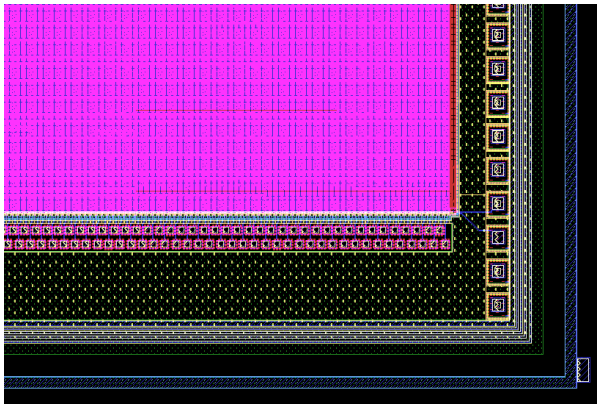
Fully Column Parallel CCD

# 3rd Generation Detector – Very Fast CCD

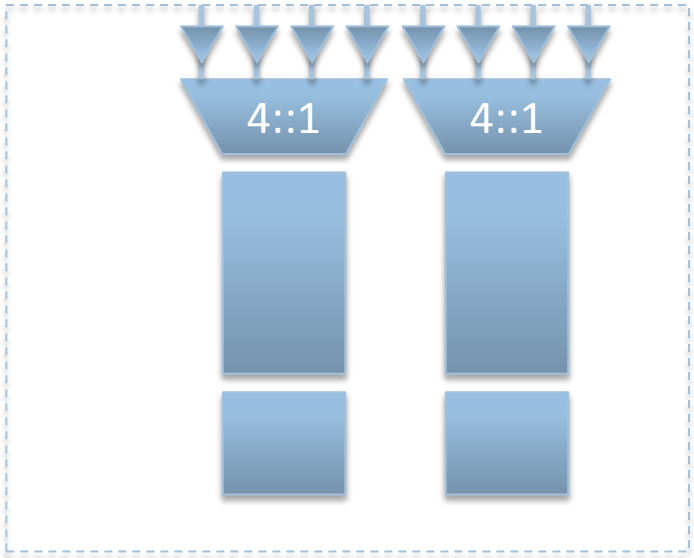


| Conventional CCD | FastCCD | Very FastCCD |
|---|---|---|
| 4-port | (almost)Column Parallel | Column Parallel |
| Commercial readout | *fCRIC* (custom 0.25 µm CMOS readout IC) | *HIPPO* (custom 65 nm CMOS readout IC) |
| $10^0$ fps | $10^2$ fps | $>10^{3.5}$ fps |

# Almost Parallel → Fully Parallel



- Still a CCD
- Limit will be $10^3$ – $10^4$ Mpix/s
  - Limited by clock rates
- 2 developments required:
- Prototype CCD – in fabrication now
- Prototype readout IC - in fabrication now

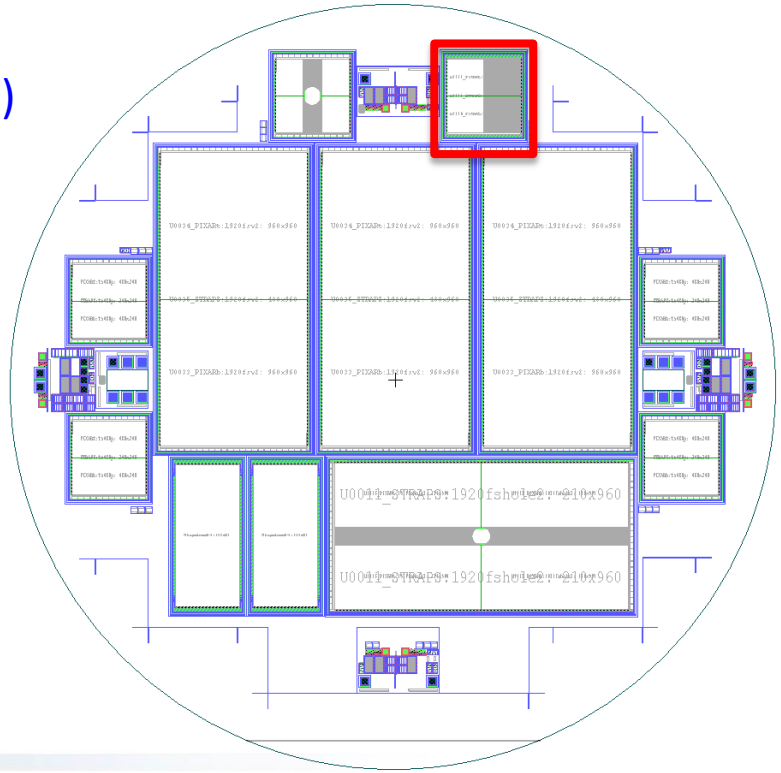



*HIPPO* 65 nm CMOS

Preamp
(multi-slope)
Mux

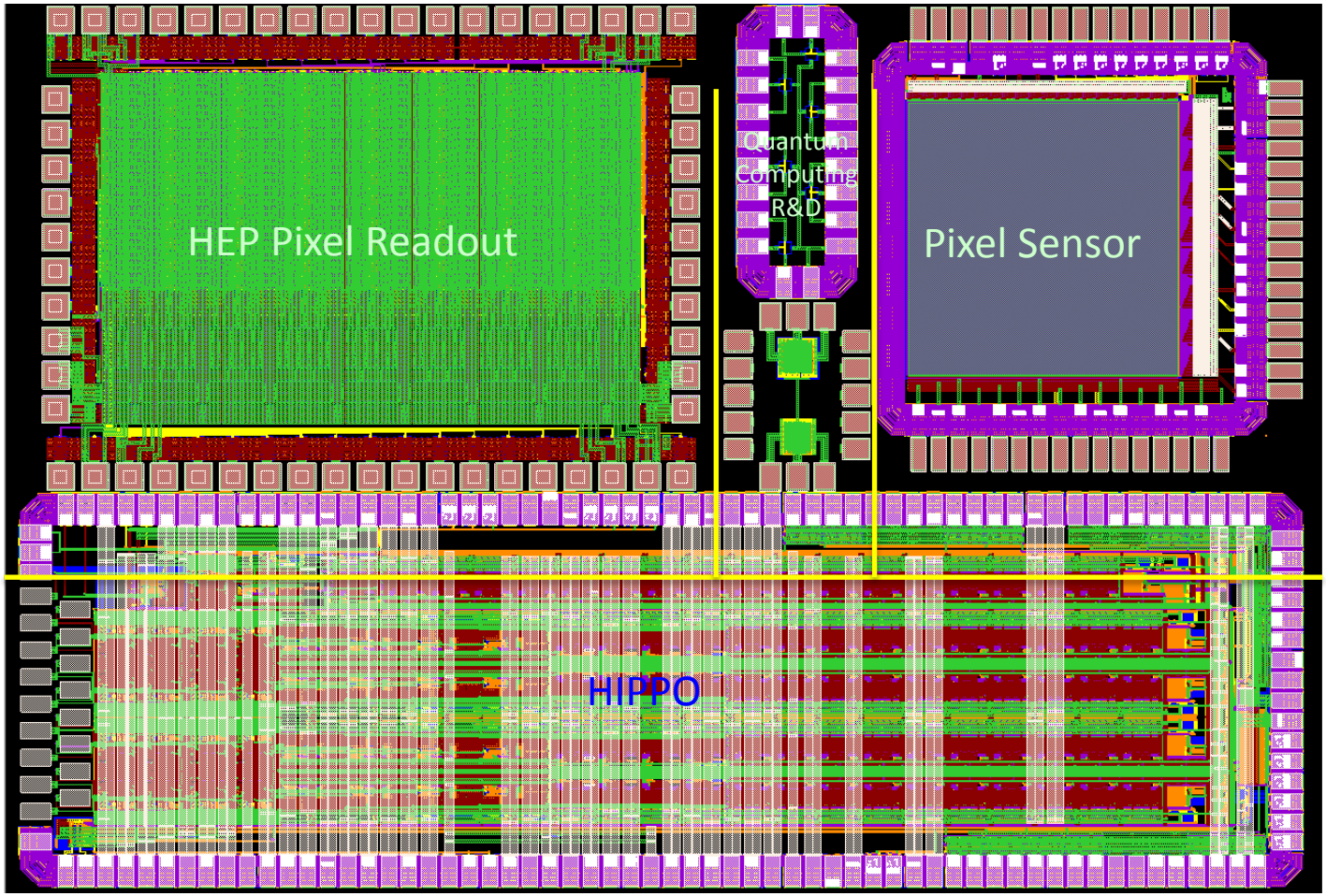
80 MHz
10-bit ADC

Serializer



# HIPPO Submission

- June 2011



# The End