

Tim Mooney, Kurt Goetze EPICS-collaboration meeting – June 15, 2018







Overview





Deployed and maintained in much the same way as a VME IOC (cross compiler, NFS mount, procServ)





Overview



- softGlueZynq enables beamline users to construct simple digital electronic circuits, and connect those circuits to field wiring, by writing to EPICS process variables (PVs).
- softGlueZynq also provides user control over how hardware interrupts are generated by field I/O signals, and dispatched to cause EPICS processing.
- softGlueZynq circuits can be autosaved and restored, saved as text files, emailed to another user, and managed by *configMenu*.
- softGlueZynq does this by loading an Xilinx Zynq FPGA with a predefined collection of circuit elements (logic gates, counters, flip-flops, etc.), whose inputs and outputs are connected to switches controlled by EPICS PVs.







MEDM display







How it works, conceptually













Circuit-element inputs



option	example	result	comment
empty		1	
number	1 0 1! 0! 0.499	1 0 Positive-going pulse Negative-going pulse 0	~3 μs ~3 μs
name	mySignal	Connected to all other inputs and output named "mySignal"	





Field I/O



- Connected just as are circuit elements
- Interrupt can drive EPICS record on rising edge.

	softGlueZynqFiel	dIO_Intxx.adl	_ ¤ ×
Field Input Bit	Interrupt-driven record INTERRUPT ON INTERRUPT, MRITE SIGNAL ENABLE VALUE VIA THIS LINK	Field Output Bit	Interrupt-driven record INTERRUPT ON INTERRUPT, WRITE SIGNAL ENABLE VALUE VIA THIS LINK
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	None None	$\begin{array}{c} = & -\frac{1}{2} & 1 & 1 \\ = & -\frac{1}{2} & 2 \\ = & -\frac{1}{3} & 3 \\ = & -\frac{1}{4} & 4 \\ = & -\frac{1}{5} & 5 \\ = & -\frac{1}{6} & 6 \\ = & -\frac{1}{7} & 7 \\ = & -\frac{1}{8} & 8 \\ = & -\frac{1}{9} & 9 \\ = & -\frac{1}{1} & 10 & 10 \\ = & -\frac{1}{1} & 11 & 11 \\ = & -\frac{1}{1} & 12 & 12 \\ = & -\frac{1}{1} & 13 & 13 \\ \end{array}$	None None
14 14 1 15 15 1 16 16 1 CONNECTOR #	None	= 1 14 14 = 15 15 = 16 16 CONNECTO	None al None al Rising al R





- Gate&Delay Generator
 - Delay a signal.
 - Optionally, specify output pulse width.
 - 20 ns time resolution (fast version has 4 ns time resolution.)



• Frequency Counter







• 16 input scaler



 8 input multichannel scaler (in progress)









- Quadrature decoder
 - Read encoder or interferometer



• Up/Dn Counter













Data-acquisition infrastructure





Used for interferometer recorder, pixelTrigger, multichannel scaler, and histogramming scaler









Histogramming Scaler

- Like a MCS, but SYNC sets current channel to 0
- 64 time bins, channel advance at up to 50 MHz (fast version up to 250 MHz)

softGlueZyng HistScal.adl _ = × tmm:softGlue: HistScal 1 EN = SYNC = = HistScal-1 DET = CLEAR. = 1

piezoDiffraction data (Phil Ryan - 6idb)





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pixelTrigger (1D fly scan)

- Track location of focal spot on sample (X_{ZP} – X_{SAMPLE})
- Generate triggers from focal spot motion.
- User specifies pixel size in interferometer ticks.













Ptychotomography measurement:

- Spiral generated by waveform generator driving piezos
- Recorded (X_{ZP}, X_{SAMPLE}, Y_{ZP}, Y_{SAMPLE}, Image number, Time)
- Interferometer at 500 Hz, camera at 20 Hz







Application

- X-ray microscope data-acquisition system (2D fly scan)
 - Trigger when focal spot leaves a pixel
 - Event data: -
 - (x,y)
 - 7 counters
 - Events at <400 kHz









Application



• pixelTrigger Demo: response to impulse







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softGlueZynq



Application

- Time resolved data acquisition (3D fly scan)
 - Trigger on pixel OR time boundary
 - Event data: -
 - (x,y)
 - ΔT since sync -
 - $dT > 2 \mu s (20 ns?)$











Application

- Time resolved data-acquisition (3D fly)
 - dT 5 μs









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