



FALL 2014 EPICS Collaboration Meeting

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CEA Saclay, France



METHODOLOGY FOR THE DEVELOPMENT OF INTELLIGENT DATA AND IMAGE ACQUISITION SYSTEMS USING **EPICS** AND **FLEXRIO** TECHNOLOGY

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GRUPO DE INVESTIGACIÓN EN
INSTRUMENTACIÓN Y
ACÚSTICA APLICADA





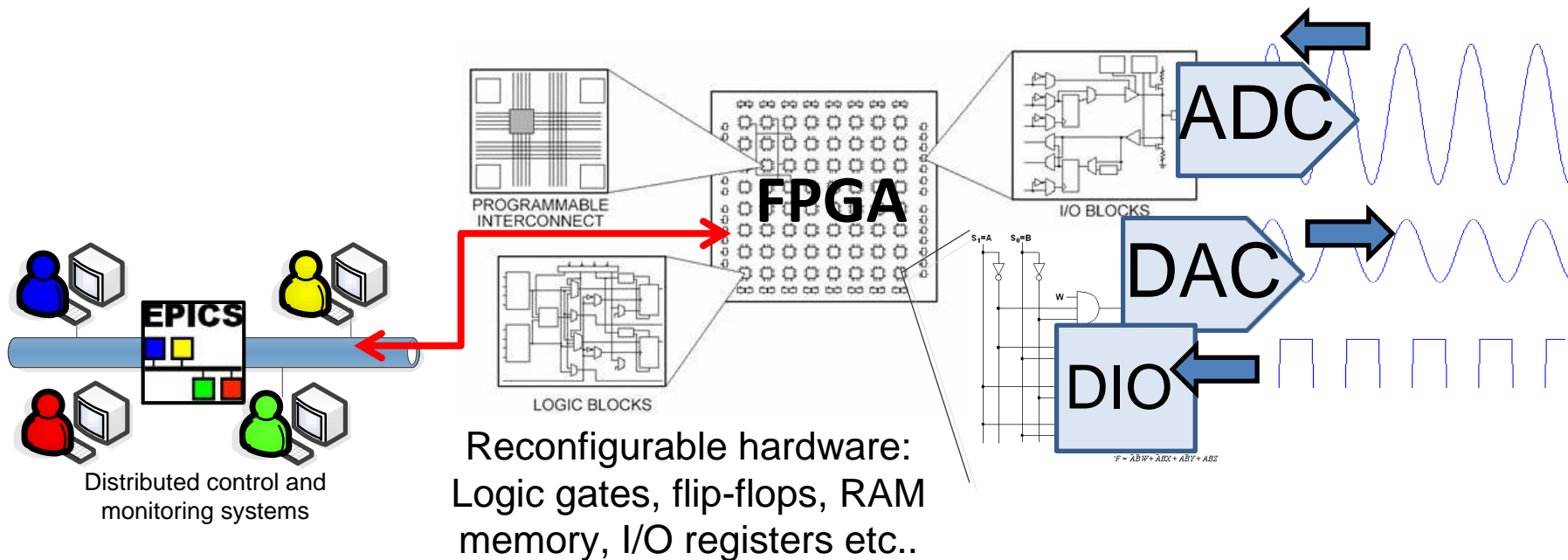
Outline

- Introduction
- RIO & FlexRIO Devices
 - Reconfigurable hardware based on FPGA
 - Interchangeable physical front ends for FlexRIO devices
- NIRIO-EPICS Device Support
 - I-RIO Driver
 - EPICS Device support for every RIO/FlexRIO configuration
- Design Methodology
 - Procedure
 - Example of FPGA implementation
- Applications
 - ITER
 - ESS Bilbao
- Conclusions
- Future works
- References



Introduction

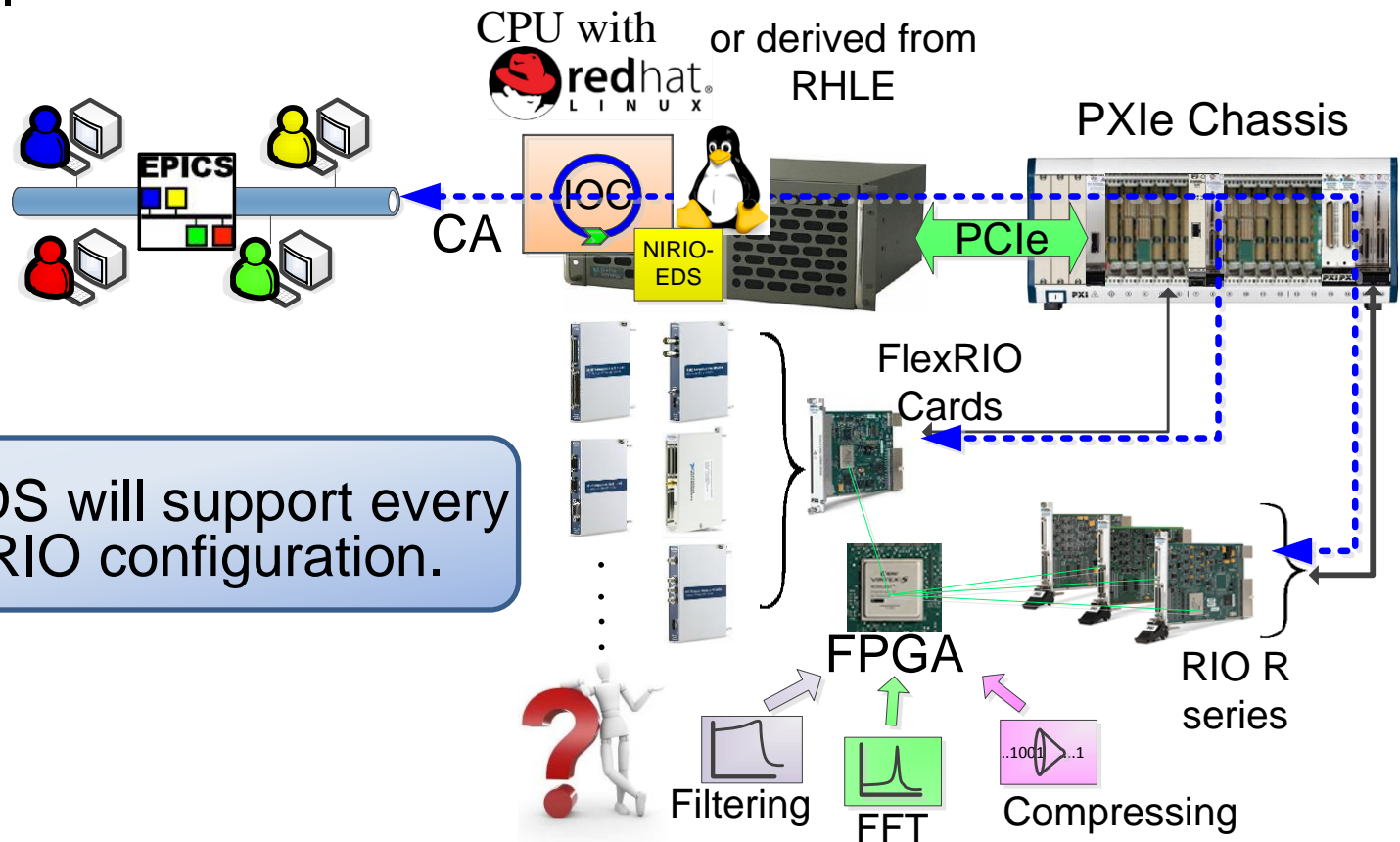
- Nowadays large scale experiments require EPICS and reconfigurable DAQ devices based on FPGA.
- EPICS provides a powerful software framework.
- FPGAs provide reconfigurable hardware with deterministic data preprocessing capabilities.





Introduction

- We propose a design methodology for **RIO/FlexRIO** devices, to be supported by a **NIRIO EPICS Device Support (NIRIO-EDS)** based on asynDriver.

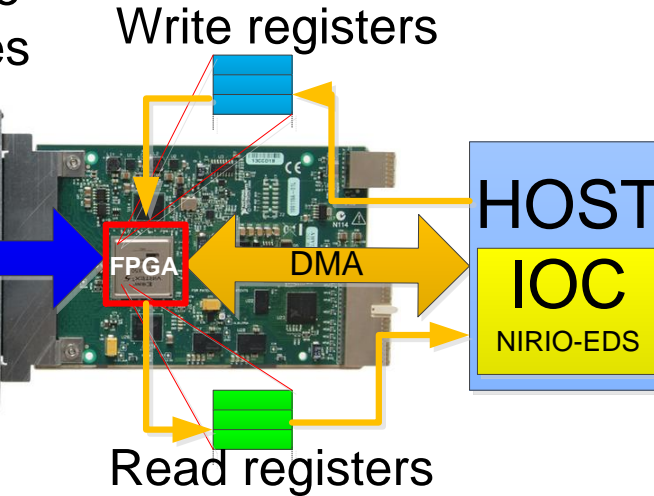
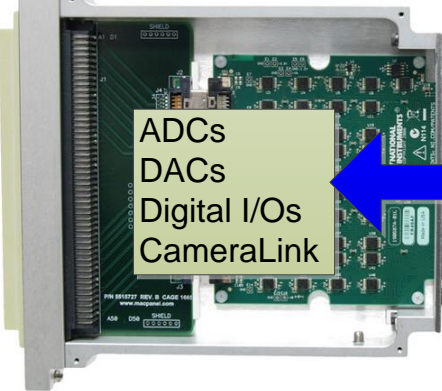
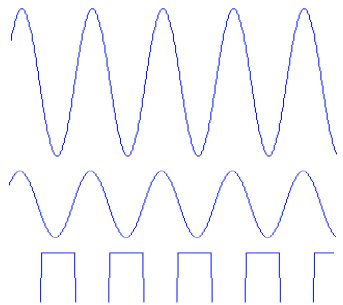


- NIRIO-EDS will support every RIO/FlexRIO configuration.



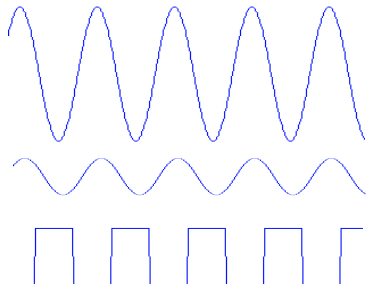
RIO/FlexRIO Devices

Interchangeable FlexRIO device Adapter modules

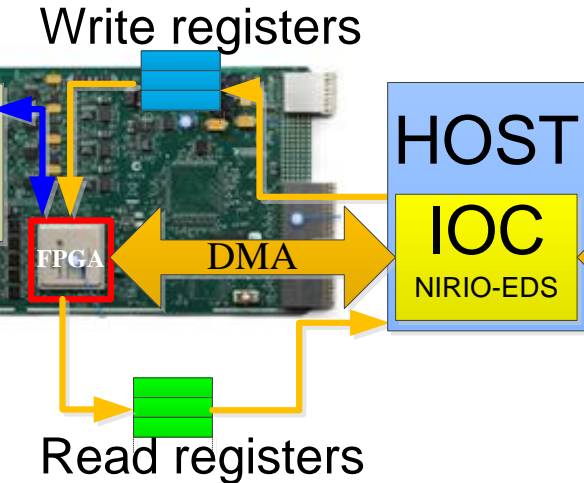
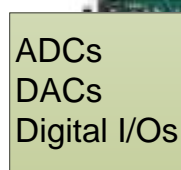


PVs
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mbbi
Mbbo
string
Waveforms
...

RIO device



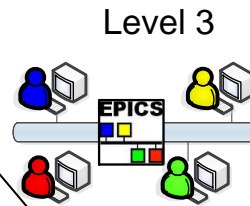
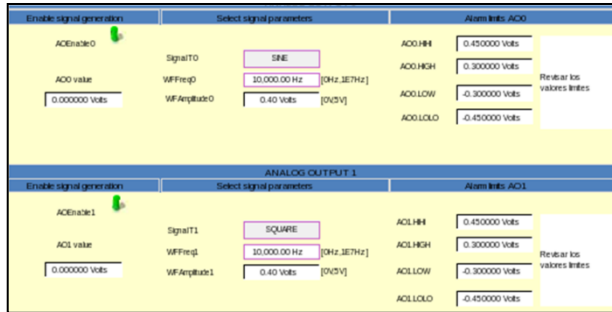
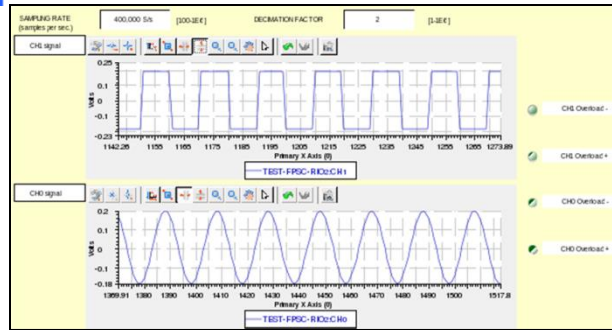
Fixed I/O



PVs
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NIRIO-EDS based on asynDriver

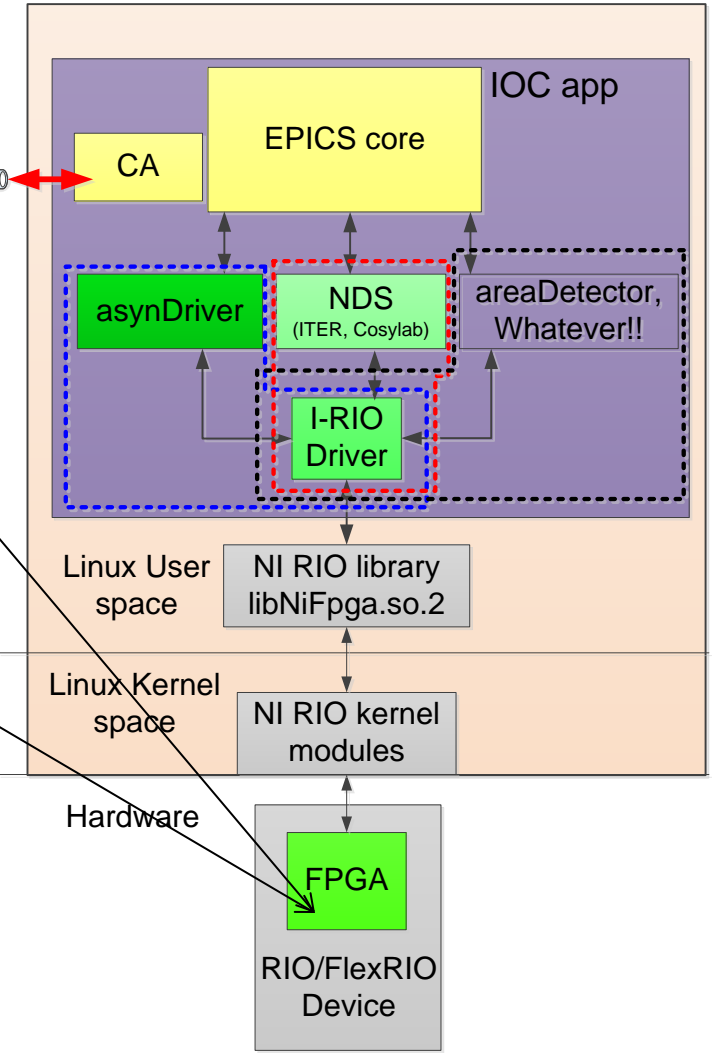


Level 2.b

Level 2.a

Level 1

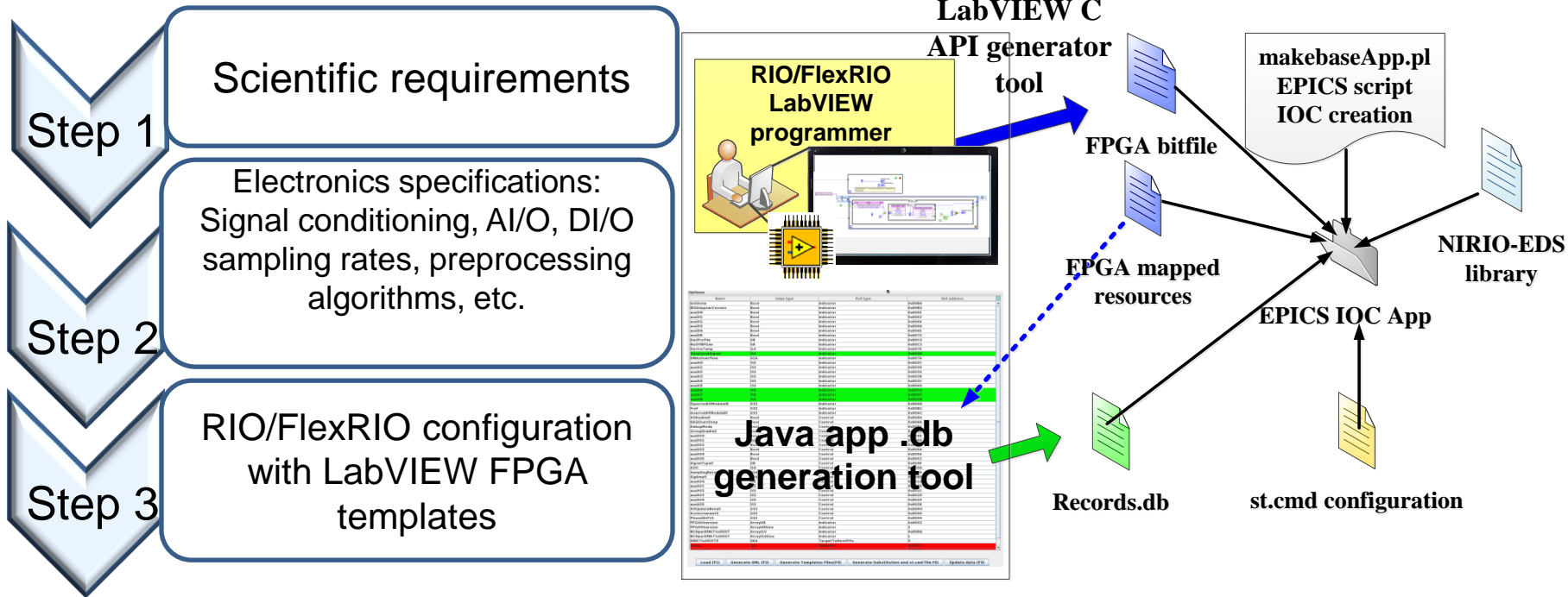
Level 0



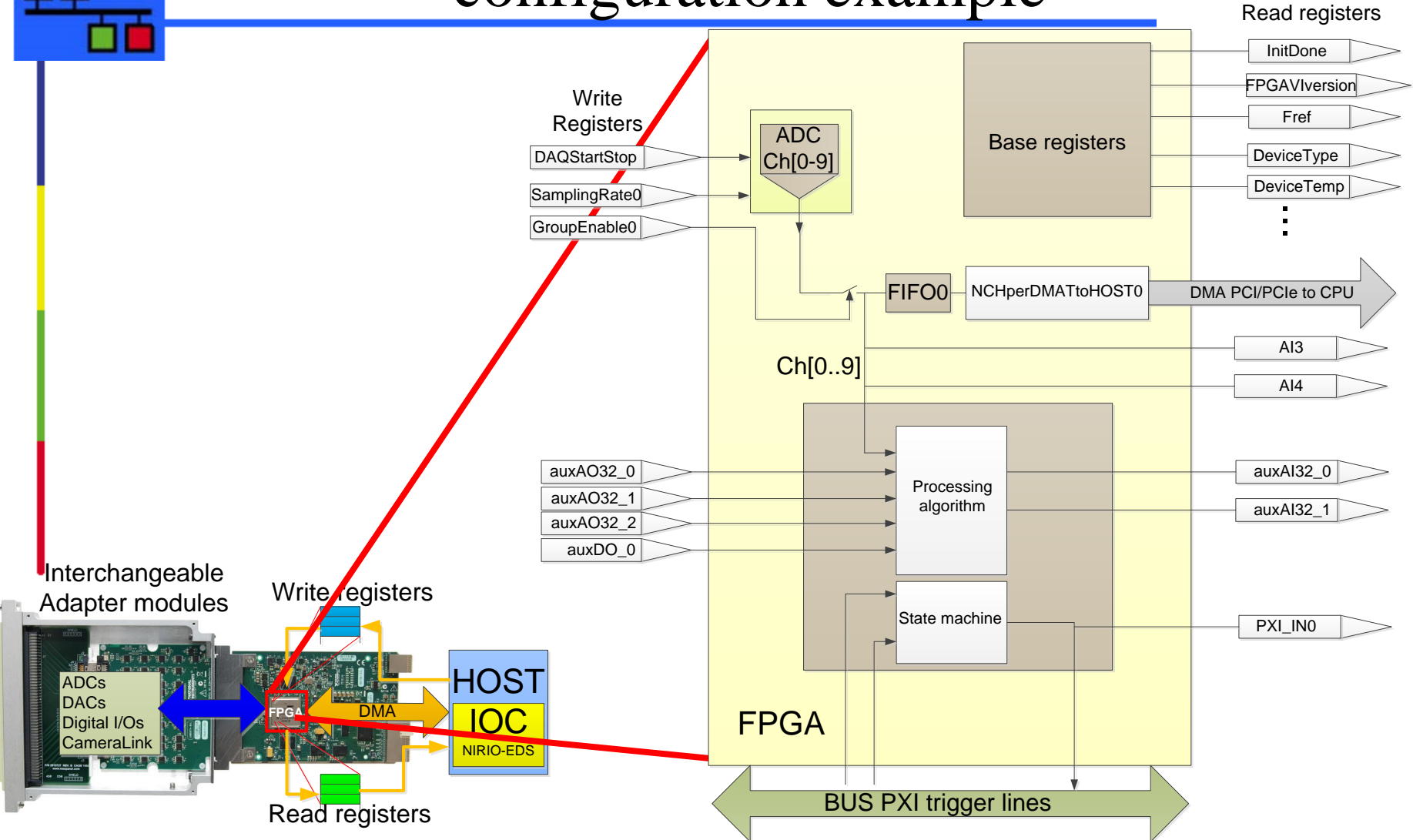
- **I-RIO Driver** detects in run time **FPGA** configuration, and **FPGA I/O registers** and **DMA** channels are dynamically interfaced with **EPICS**.

Design Methodology for RIO/FlexRIO devices

- Records database file is **generated automatically** using FPGA mapped resources. Including all files in EPICS software unit, the IOC is ready to control & monitor the RIO/FlexRIO

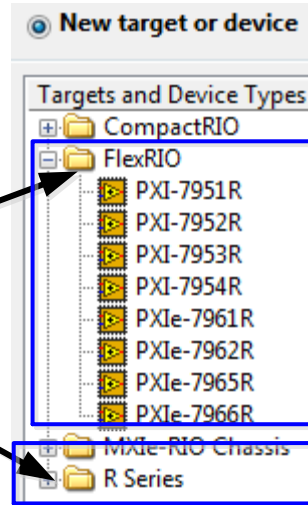
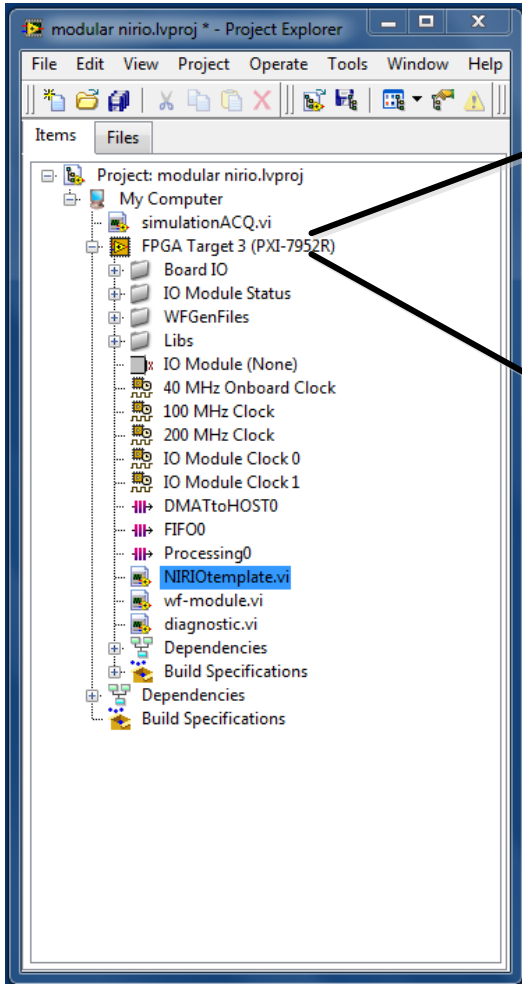


FPGA (RIO/FlexRIO) configuration example





FlexRIO configuration



FlexRIO configuration

Step 1. Fill each of the next fields according to the required DAQ implementation.

FPGAVersion 1.a. Introduce the firmware version for this implementation.
0 1 0 U8

Fref 1.b. Introduce the reference time clock for the DAQ acquisition module.
100000000 U32

DevProfile 1.c. Available profiles: DAQ-->0; IMAQ-->1
0 U8

NCHperDMATtoHOST 1.d. Number of channels per DMA.
0 12 U16

NoOfWFGen 1.e. Introduces the number of wave form generators
1 U8

1.f. If FlexRIO adapted module is required, then configure "TRUE" this constant, it is required include the IO Module\Initialization replace for the true constante. If not configure it "FALSE"

Expected IO Module ID U32
Inserted IO Module ID U32
RIOAdapterCorrect TF

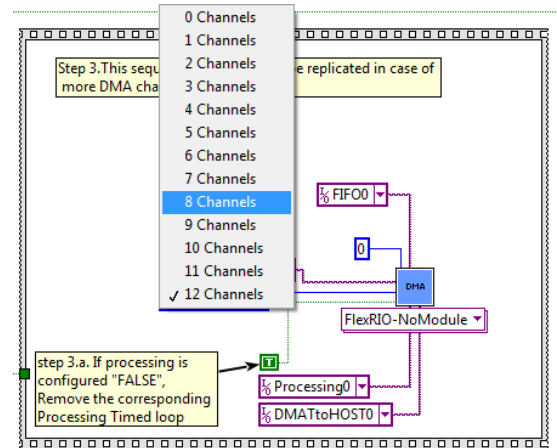
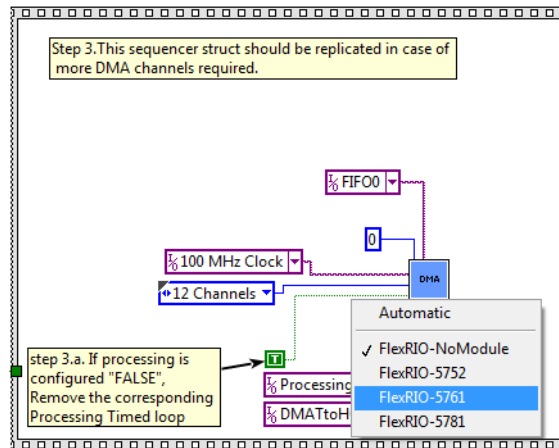
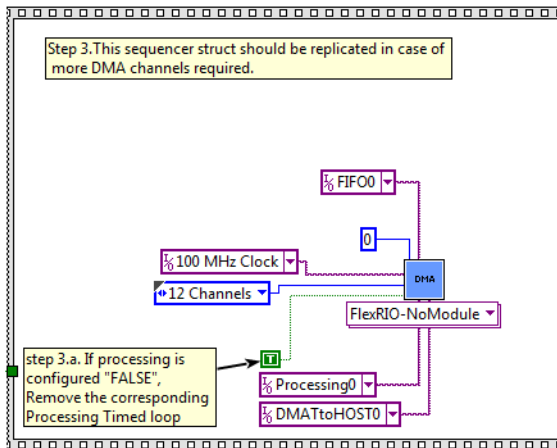
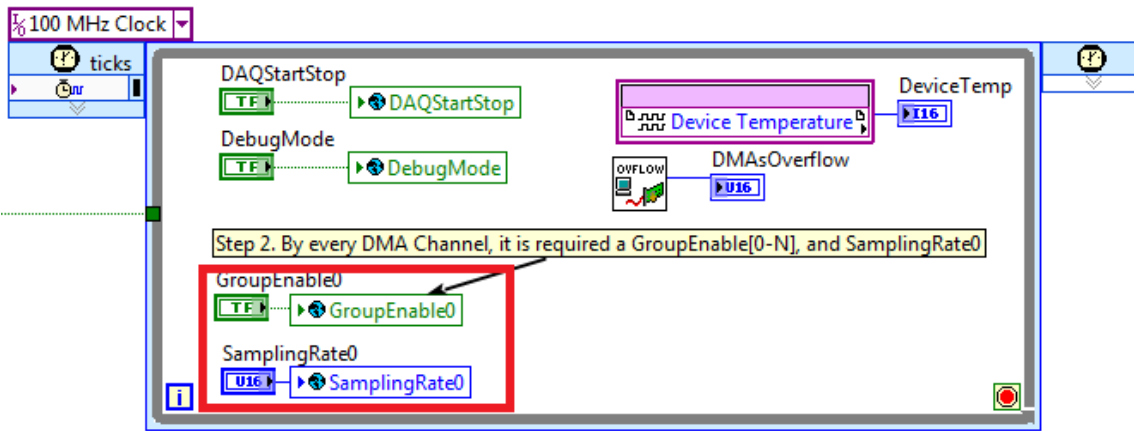
1.g. Introduce "here below" the FIFO Clear method used in all the project, and select "Clear" method for every FIFO used in the FPGA design

FIFO Clear
Processing0 Clear

InitDone TF

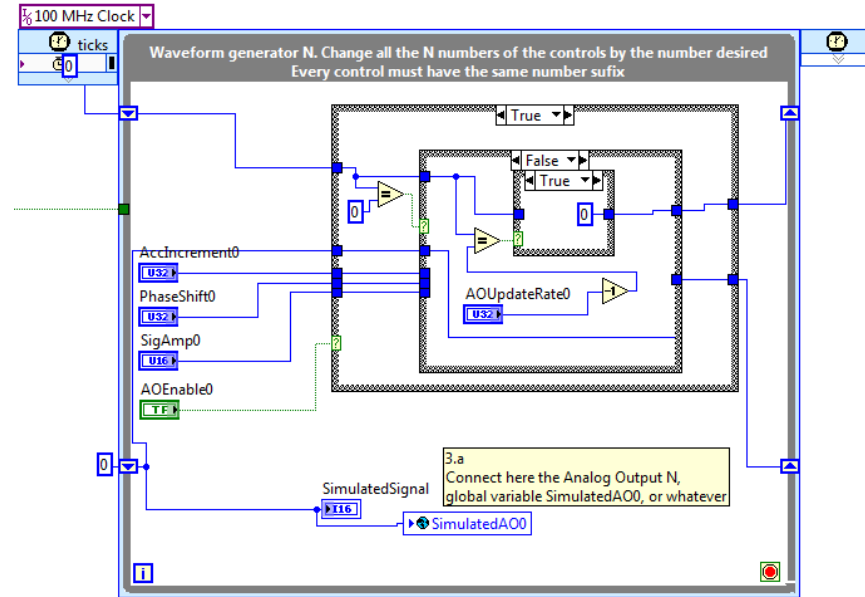
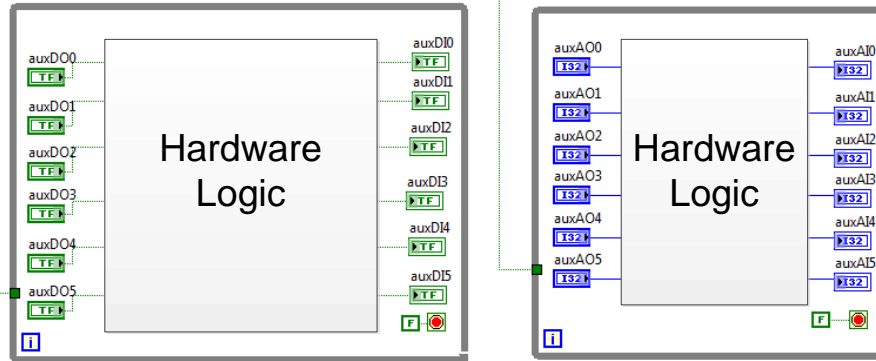


FlexRIO configuration

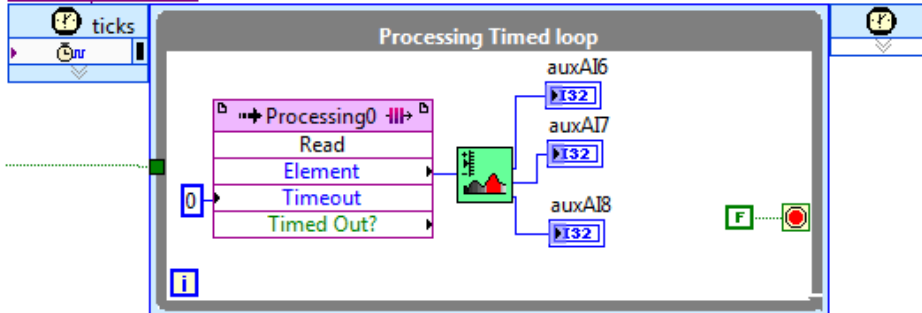


FlexRIO configuration

Step 4. Add every hardware logic algorithm, processing, using auxiliar I/O registers, using name convention



Step 5. If is programmed Processing, It is possible to use this timed loop for data processing





Use case applications

- ITER PXIe Fast controller prototype for data and Image acquisition (cameralink).

The Mini-CODAC interface displays several key components:

- System Monitoring:** A table showing the status of various FFSIC (Fast Front-End Signal Interface Controller) modules.

Module	Value	Module	Value
FFSIC Cable board	1.0	TEST-FFSIC-LPT	00:01:00
FFSIC Cable reader	29.2632%	TEST-FFSIC-BRCTME	15.0
FFSIC main switch	TEST-FFSIC-CPUAUT	TEST-FFSIC-CPUINT	16.0
FFSIC current transformer status	TEST-FFSIC-LOAD	TEST-FFSIC-RECC	28646.0
FFSIC temperature status	1.6289506737843	TEST-FFSIC-RECC	196.0
FFSIC circuit breakers AC230	88.0	TEST-FFSIC-STTOD	11:04Z011 19-14
FFSIC circuit breakers 240C1U1	TEST-FFSIC-HB	TEST-FFSIC-MEMAUT	0.8325%
FFSIC circuit breakers 240C2U2	TEST-FFSIC-MEMAUT	TEST-FFSIC-SVPORT	5064
FFSIC temperature alarm	TEST-FFSIC-MEMCNT	TEST-FFSIC-STOP	0.0
FFSIC temperature alarm	TEST-FFSIC-MEMMAX	TEST-FFSIC-LOCKET	19.0
- Data Acquisition:** Multiple 'Signals DMA0' plots showing waveforms for different channels (e.g., TEST-FFSIC-RX02-CH0, TEST-FFSIC-RX02-CH1).
- Setup FLEXRIO0-P017854:** Configuration parameters for the FlexRIO board, including 'start data acquisition', 'Decimation Factor Group 0' (1.00), 'DMA0 Enable', and 'Sampling Rate (p-11)' (750.000.00).
- Mini-CODAC:** A central image of the physical PXIe controller hardware.
- Setup PXI7851R:** Configuration parameters for the PXI-7851R board, including 'start data acquisition', 'Decimation Factor Group 0' (1.00), 'DMA0 Enable', and 'Sampling Rate (p-11)' (750.000.00).

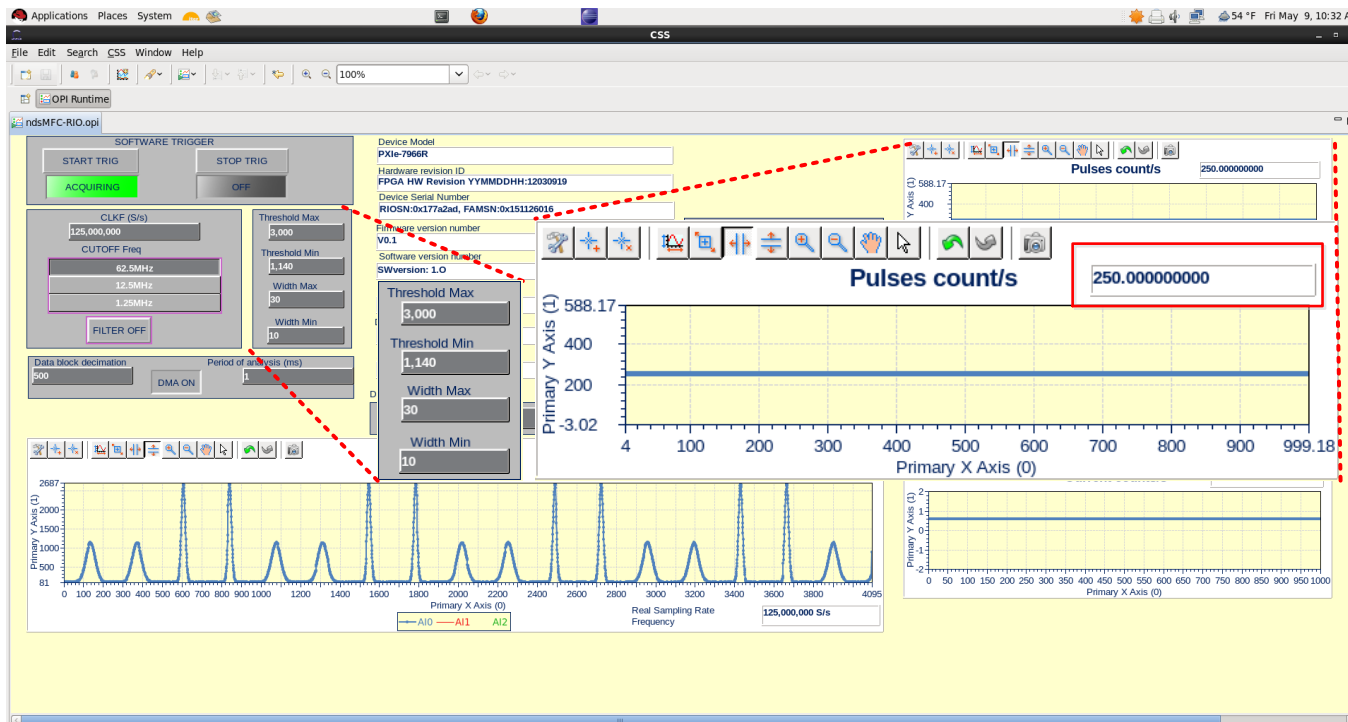
The NI RIO CAMERA LINK 1483 interface provides camera control and monitoring:

- FPGA STATUS:** Shows 'FPGA Initialization OK', 'Ready to Start Acquisition', 'ERROR NUMBER: 0', 'BITFILE VI VERSION: V2.14', and 'FPGA TEMPERATURE: 33.75°C'. FIFOs 16 and 64 are marked as OK.
- CAMERA:** Includes 'Insert commands for camera configuration', 'Camera #00139-B2.04-V1.03-F1.07-G1.0', and 'Camera response:'. It also shows 'STATUS: OK', 'WATTS: 4.383 W', 'AMPERS: 0.379 A', 'VOLTS: 12.025 V', and 'TEMPERATURE: 30.00°C'.
- IMAO ACQUISITION CONTROLS:** Features 'START', 'STOP', and 'Sync' buttons.
- Video Feed:** A live camera view showing a rack of Hirschmann MA1040 modules with a vertical scale on the right ranging from -250 to 200.



Use case applications

- ITER Fission chamber diagnostic use case application based on FlexRIO technology: It integrates deterministic diagnostic into the FPGA (4 ADC sampling at 125MS/s). Processing to obtain counts, RMS and cambelling implemented in the FPGA.





Use case applications

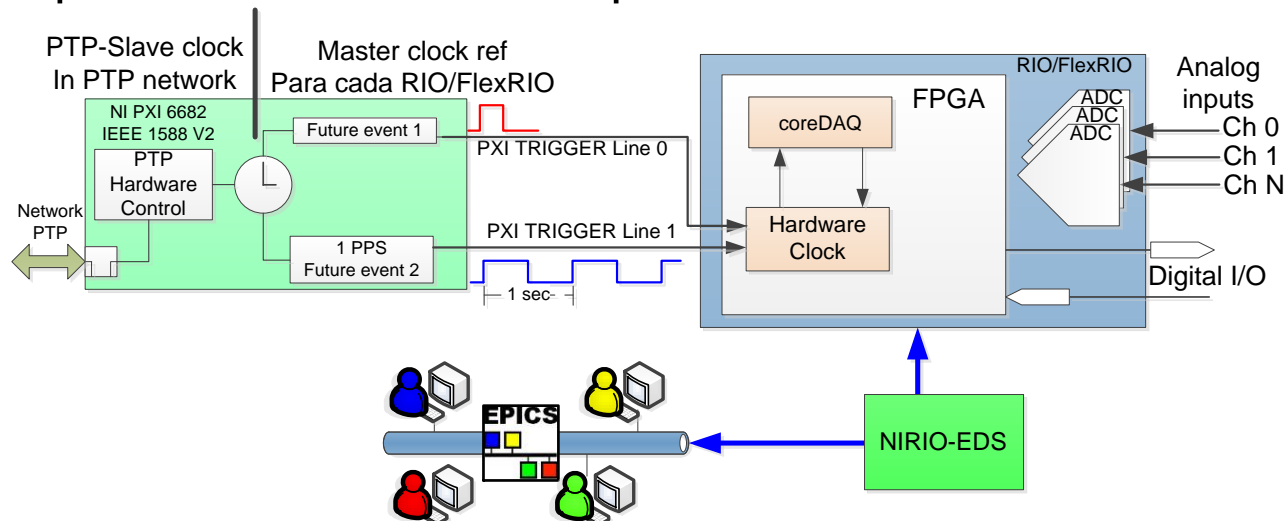
- ESS Bilbao. NIRIO-EDS will support the RIO PXI-7852R for the control and monitoring of the Ion Source Hydrogen Positive (ISHP).





Other Applications

- Integration of Hardware clock into the RIO/FlexRIO devices synchronized with IEEE1588-V2 (tenth of nanoseconds accuracy)
 - It allows real-time timestamping in the DAQ for all acquired data (or blocks) without CPU intervention. Very useful for timestamped data streaming.
 - It requires a PXI device compliant with PTP-V2.





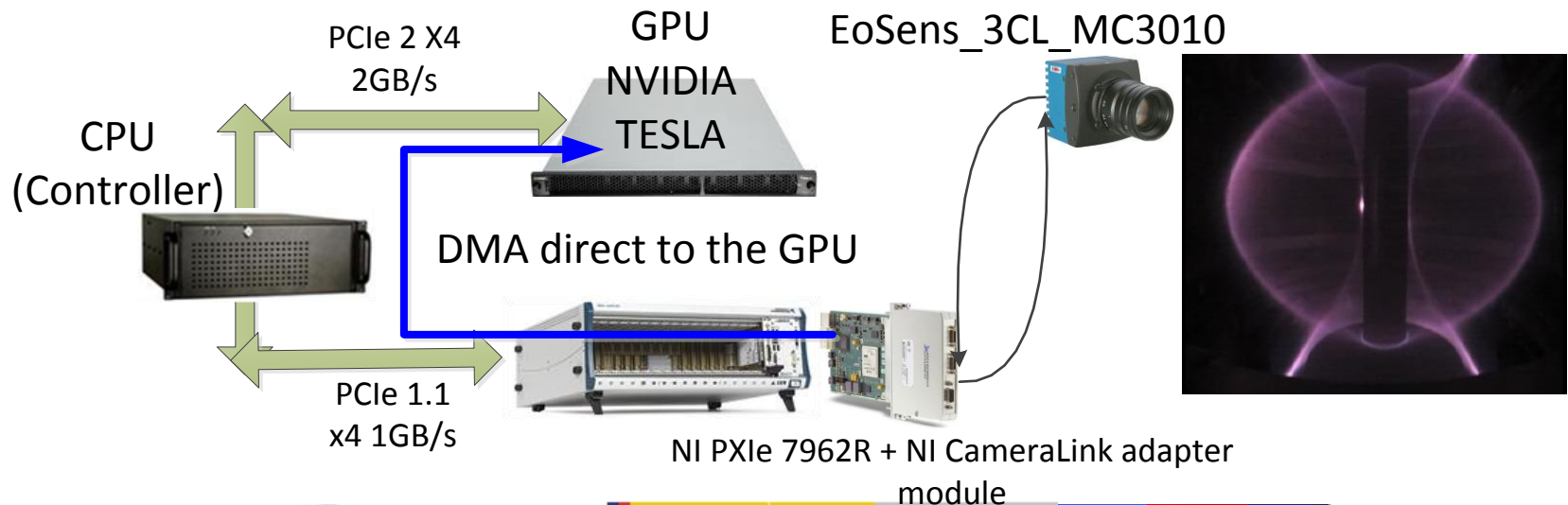
Conclusions

- We have defined a design methodology for implementing intelligent data and image acquisition into RIO/FlexRIO devices, supported by the NIRIO-EDS.
- We have developed LabVIEW patterns and libraries, that permit configure RIO/FlexRIO devices in an easy way.
- The NIRIO-EDS will support every RIO/FlexRIO configuration (implementation), without rewriting the device support.



Next Steps

- We will communicate soon to EPICS community the availability of this EPICS device support, and all RIO/FlexRIO hardware description templates and libraries (in LabVIEW for FPGA code).
- We are implementing direct data transfer communication among FlexRIO devices and GPUs without CPU intervention. This application will also include an EPICS device support to use the GPU.

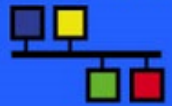


**EPICS**

References

- [1] D. Sanz, M. Ruiz, R. Castro, J. Vega, J. M. Lopez, E. Barrera, N. Utzel and P. Makijarvi, "Implementation of Intelligent Data Acquisition Systems for Fusion Experiments Using EPICS and FlexRIO Technology," *Nuclear Science, IEEE Transactions on*, vol. 60, pp. 3446-3453, 2013.
- [2] D. Sanz, M. Ruiz, J. M. Lopez, R. Castro, J. Vega and E. Barrera, "IEEE 1588 clock distribution for FlexRIO devices in PXIe platforms," *Fusion Eng. Des.*, vol. 89, pp. 652-657, 5, 2014.
- [3] E. Barrera, M. Ruiz, D. Sanz, J. Vega, R. Castro, E. Juárez and R. Salvador, "Test bed for real-time image acquisition and processing systems based on FlexRIO, CameraLink, and EPICS," *Fusion Eng. Des.*, vol. 89, pp. 633-637, 5, 2014.

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Thank you very much for your attention!!
questions?



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