



國家同步輻射研究中心
National Synchrotron Radiation Research Center



Timing Solution for the TPS Project

< EPICS Collaboration Meeting Fall 2012 >

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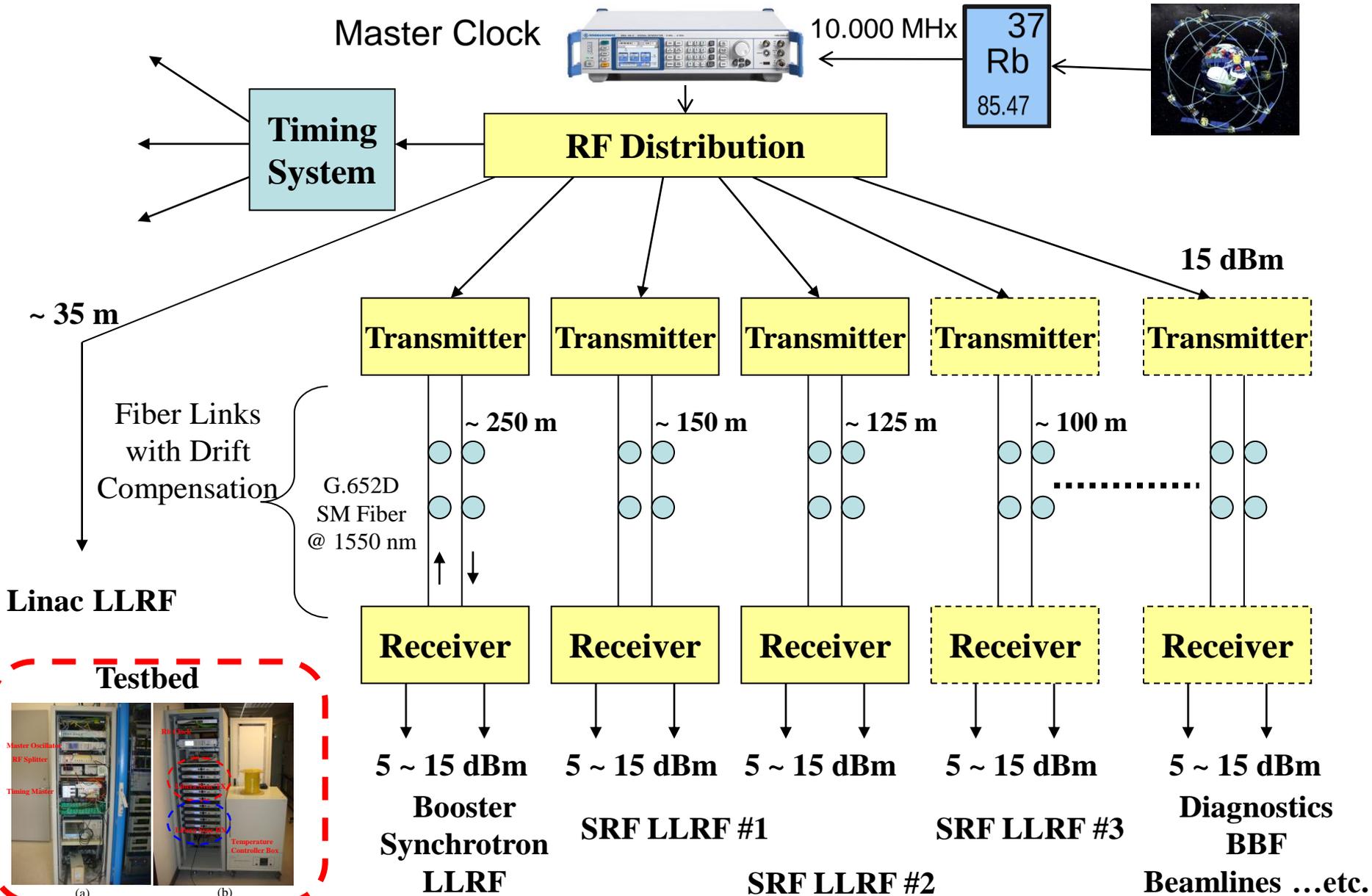
NSRRC



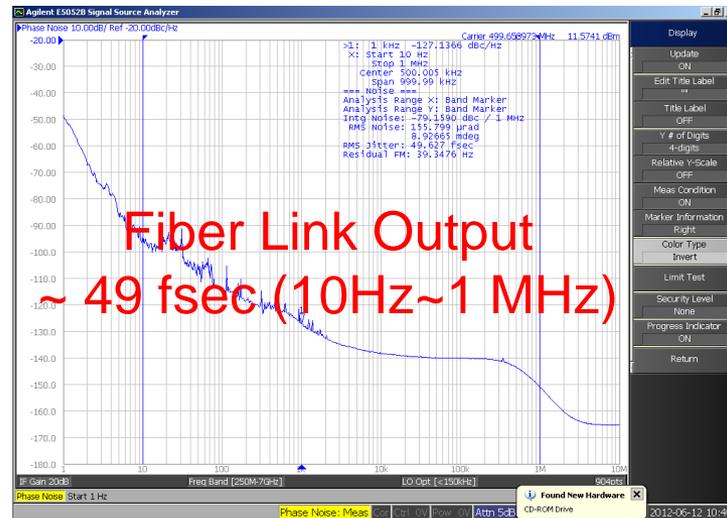
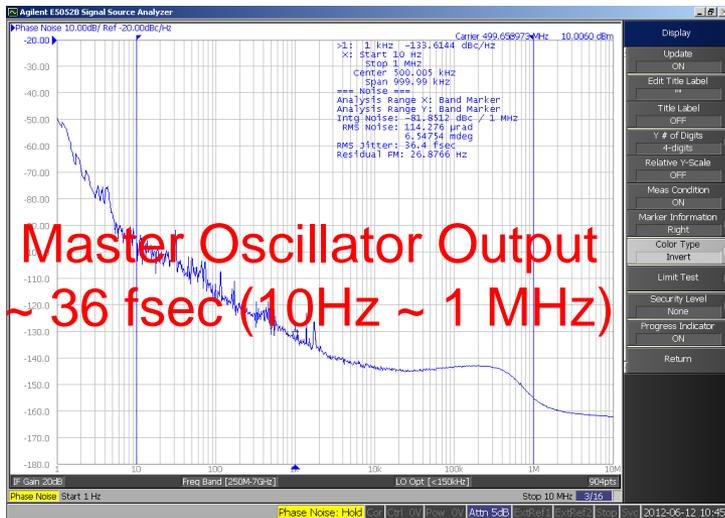
Outline

- TPS RF reference distribution
- TPS timing system
 - Hardware
 - Timing system distribution network
 - Timing system diagnostic
- Sequence RAM management
- Summary

TPS RF Reference Distribution

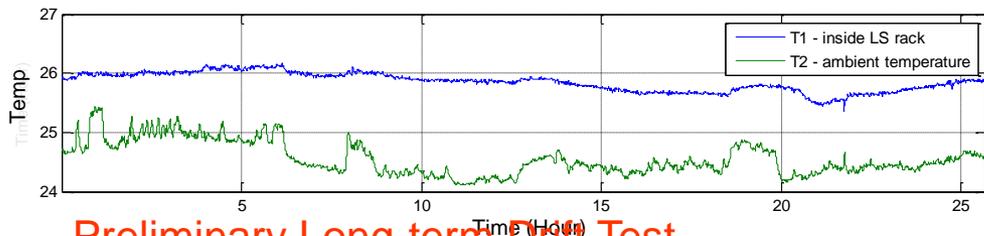


RF Reference Distribution - Performance Test



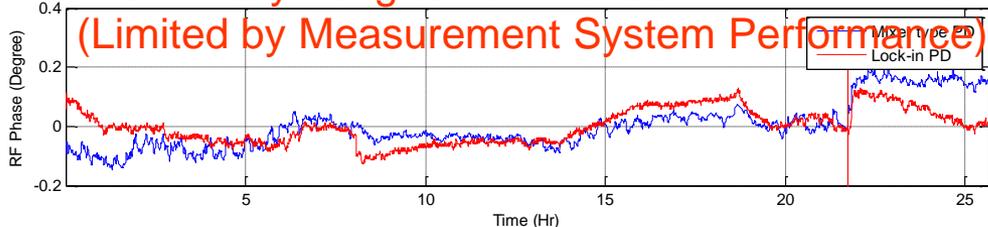
Added Jitter = $\text{SQRT}(49^2 - 36^2) \sim 33 \text{ fsec}$ ($\ll 0.1^\circ$ RF phase at 500 MHz)

It's sufficient for TPS RF stability requirement



Preliminary Long-term Drift Test

(Limited by Measurement System Performance)



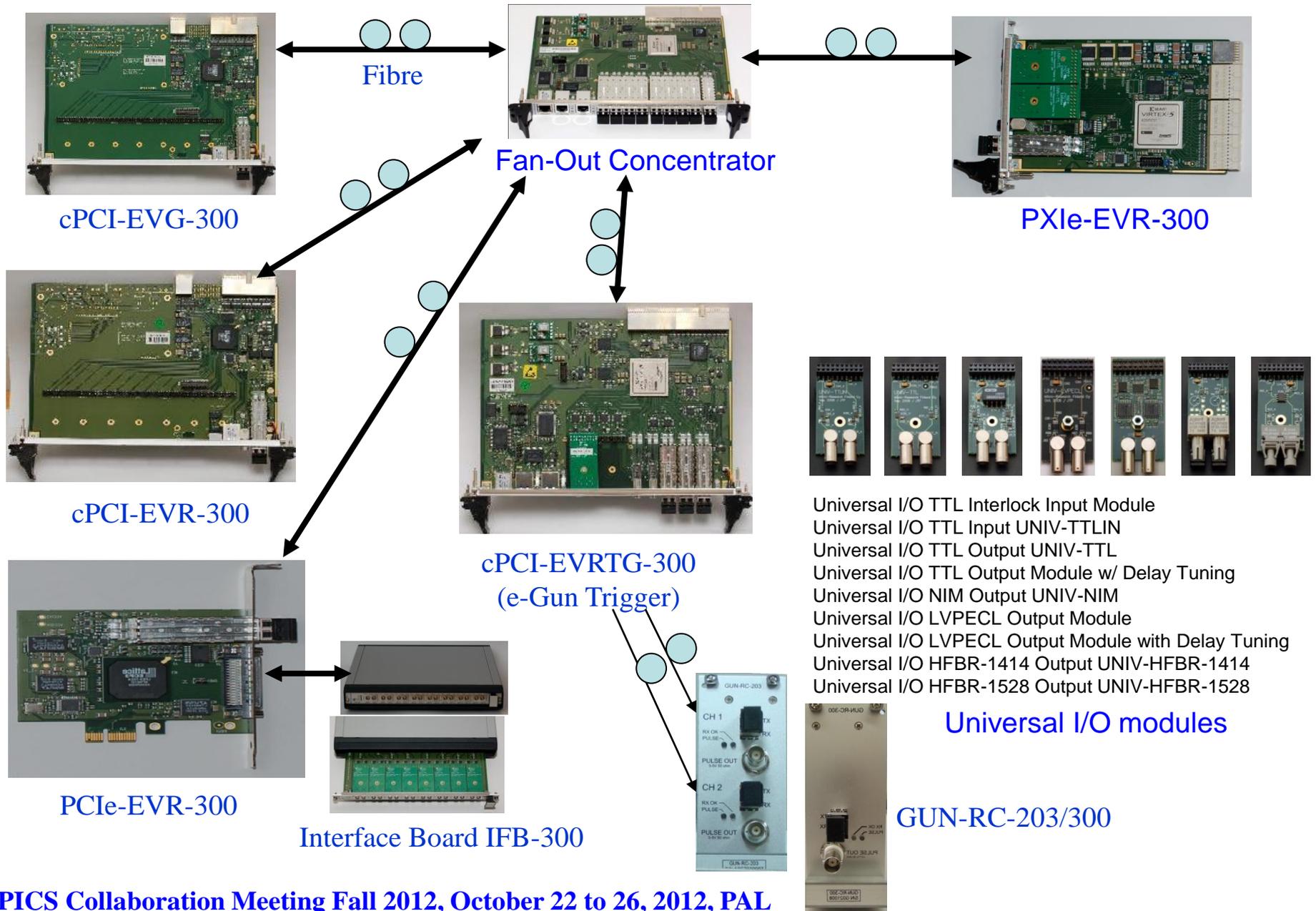
(a)

(b)

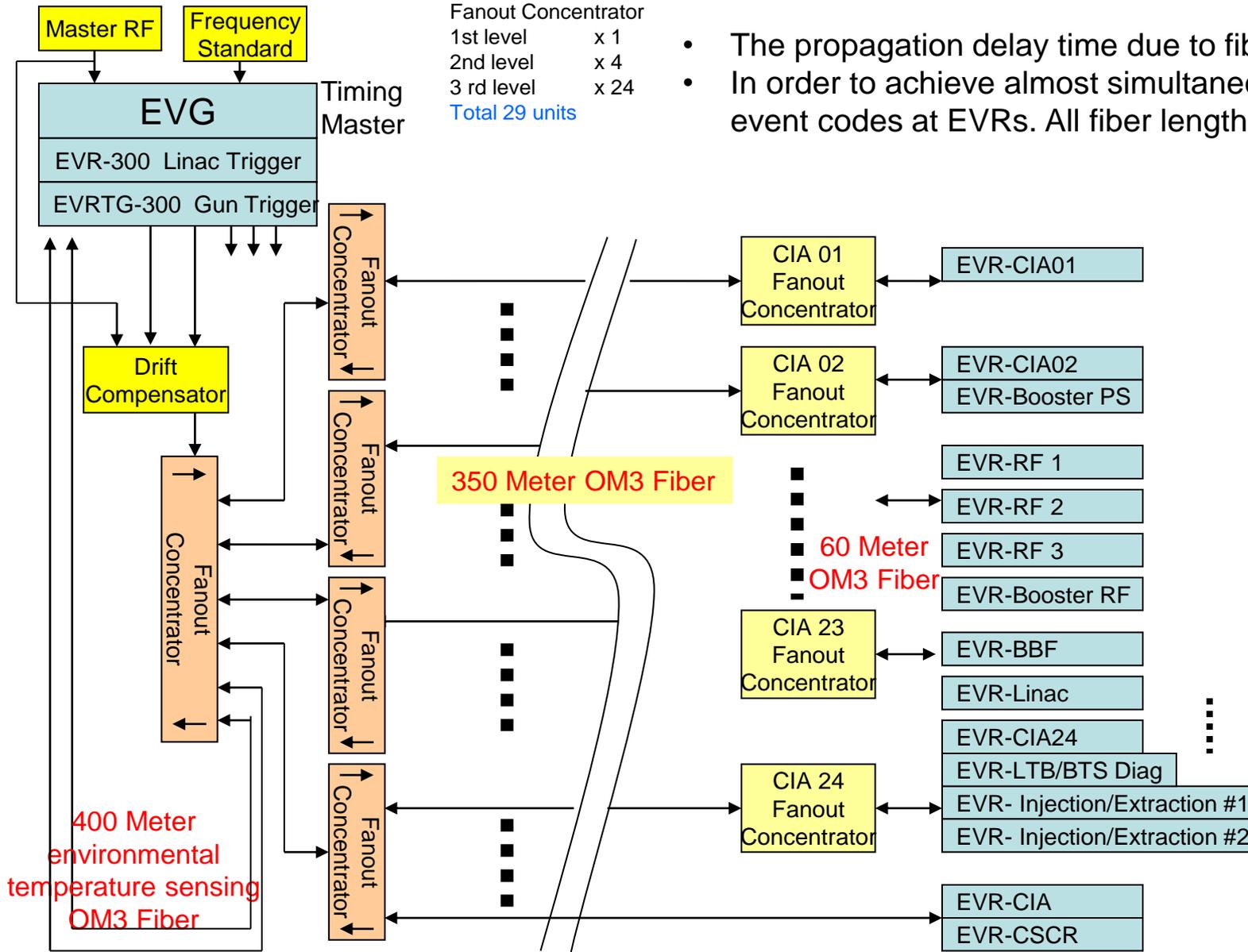
Timing System Solution

- Main Parameters
 - RF : 499.654 MHz
 - Booster revolution clock : 603.445 kHz (864 bucket)
 - Storage ring revolution clock : 578.303 kHz (828 bucket)
 - Coincidence clock : 25.14 kHz
 - Event Clock : 124.9135 MHz
 - Jitter : < 20 ps (cPCI-EVR), < 10 ps (cPCI-EVRTG)
 - Resolution : 8.0054 ns
 - Repetition rate : 3 Hz
- Hardware form fact
 - 6U compactPCI
 - EVG
 - EVR
 - EVRTG
 - Fan-Out Concentrator
 - PCIe
 - EVR
 - PXIe
 - EVG (available in the mid of next year, R&D purpose for possible TLS upgrade)
 - EVR

Timing System Hardware



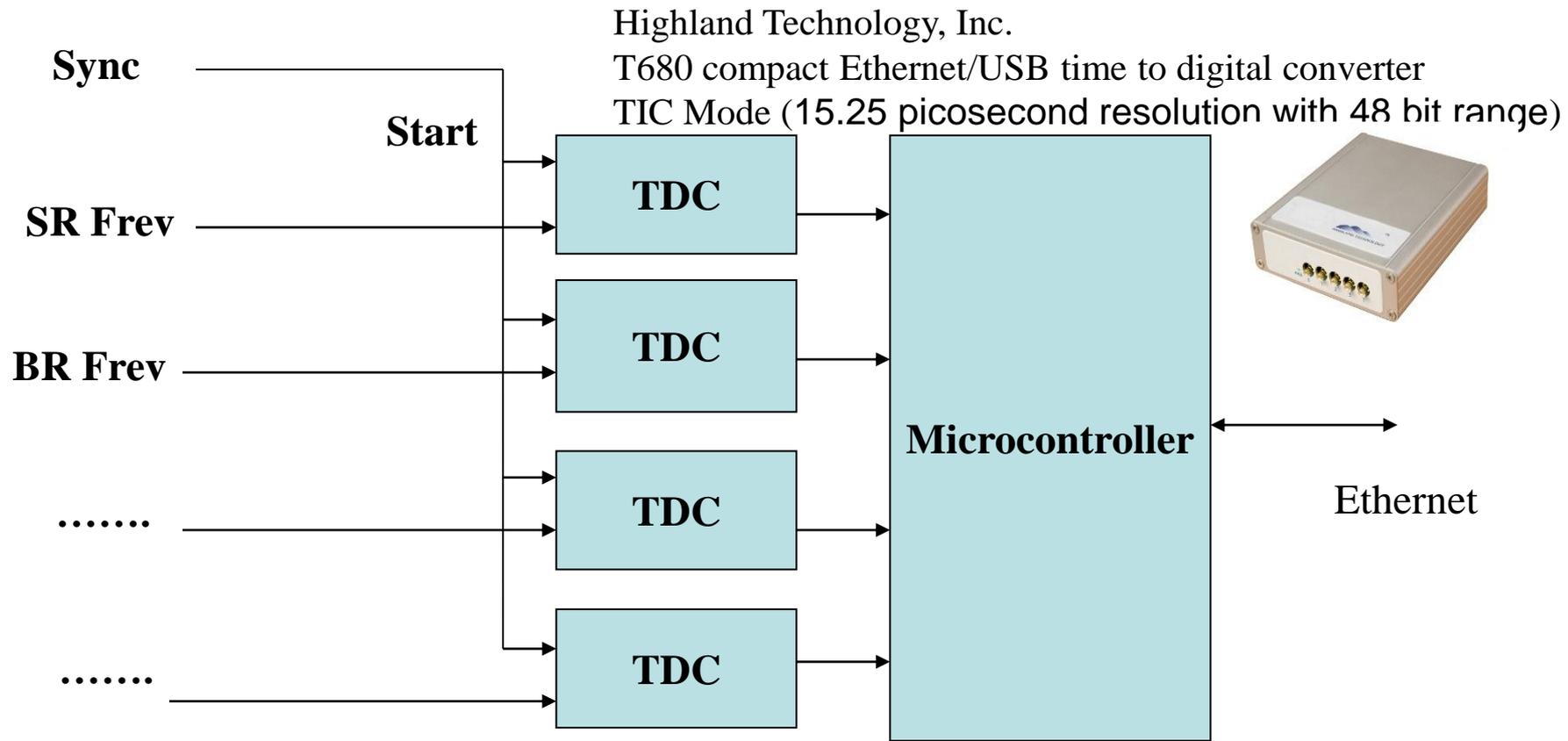
Timing System Distribution Network



- The propagation delay time due to fiber is ~5 ns/m.
- In order to achieve almost simultaneous receipt of event codes at EVRs. All fiber lengths are equal.

Timing System Health Monitoring

(TDC + Oscilloscope + Lock-in Amplifier)



Oscilloscope
(waveform observation)



High frequency Lock-in Amplifier
(drift measurement)

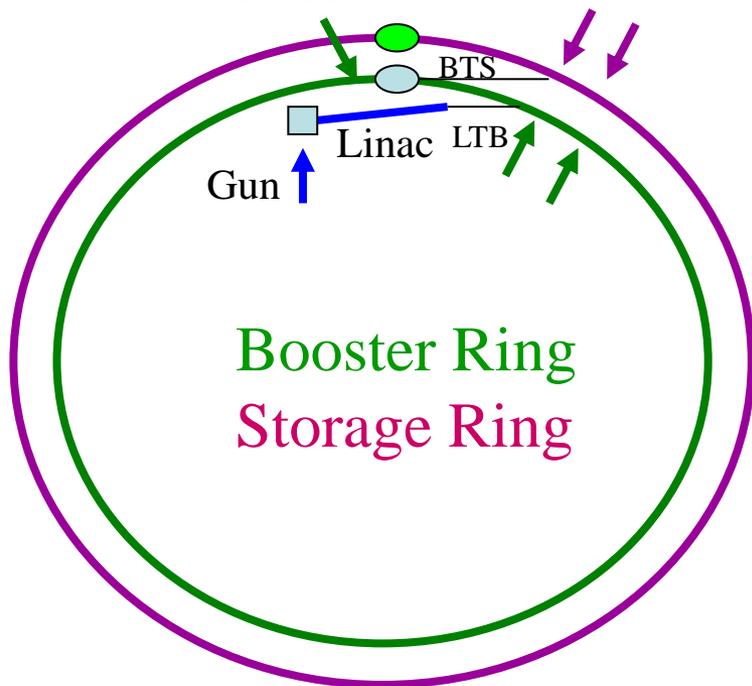
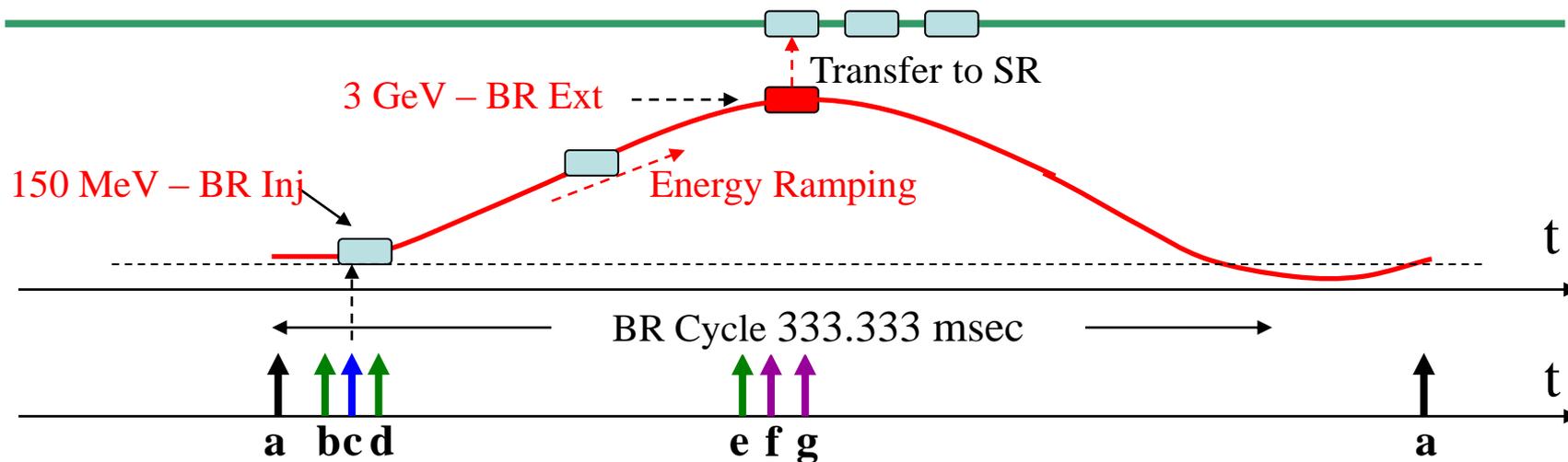
What operation mode will be delivered in timing system?

- Various operation mode
 - Accelerator subsystem test mode
 - Individual subsystem(or devices) trigger control for debug mode
 - Bunch mode selection
 - Single shot injection
 - Continue injection
 - Repetitive rate decimation for specific trigger.
 - Warm up trigger for specific device.
 - Bucket addressing.
 - Top-up injection for desired fill pattern.
 - Top-up injection with filling pattern feedback.
 -

How to handle these operation modes?

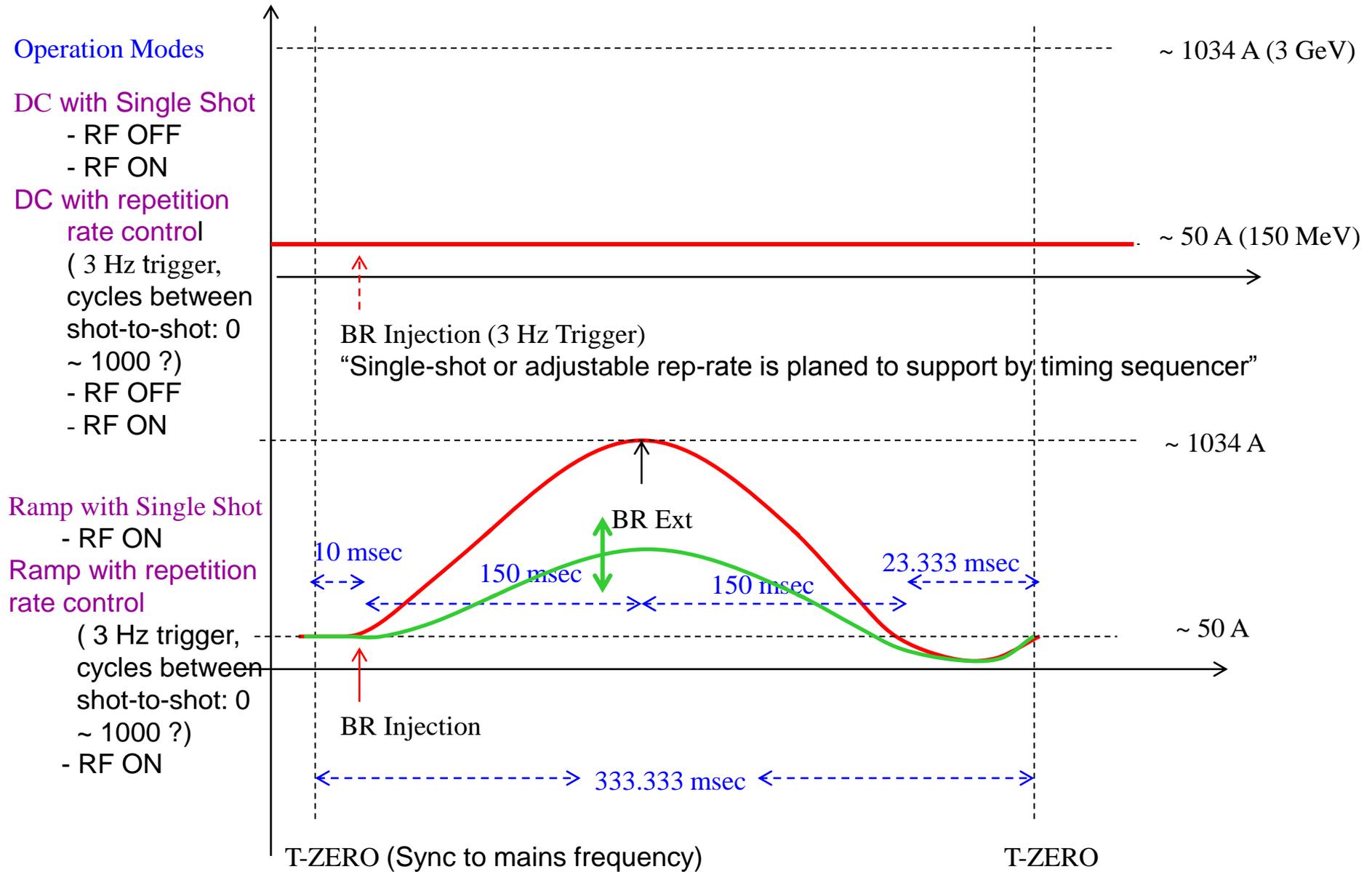
=> By well managing sequence RAM of EVG

Example of reference events

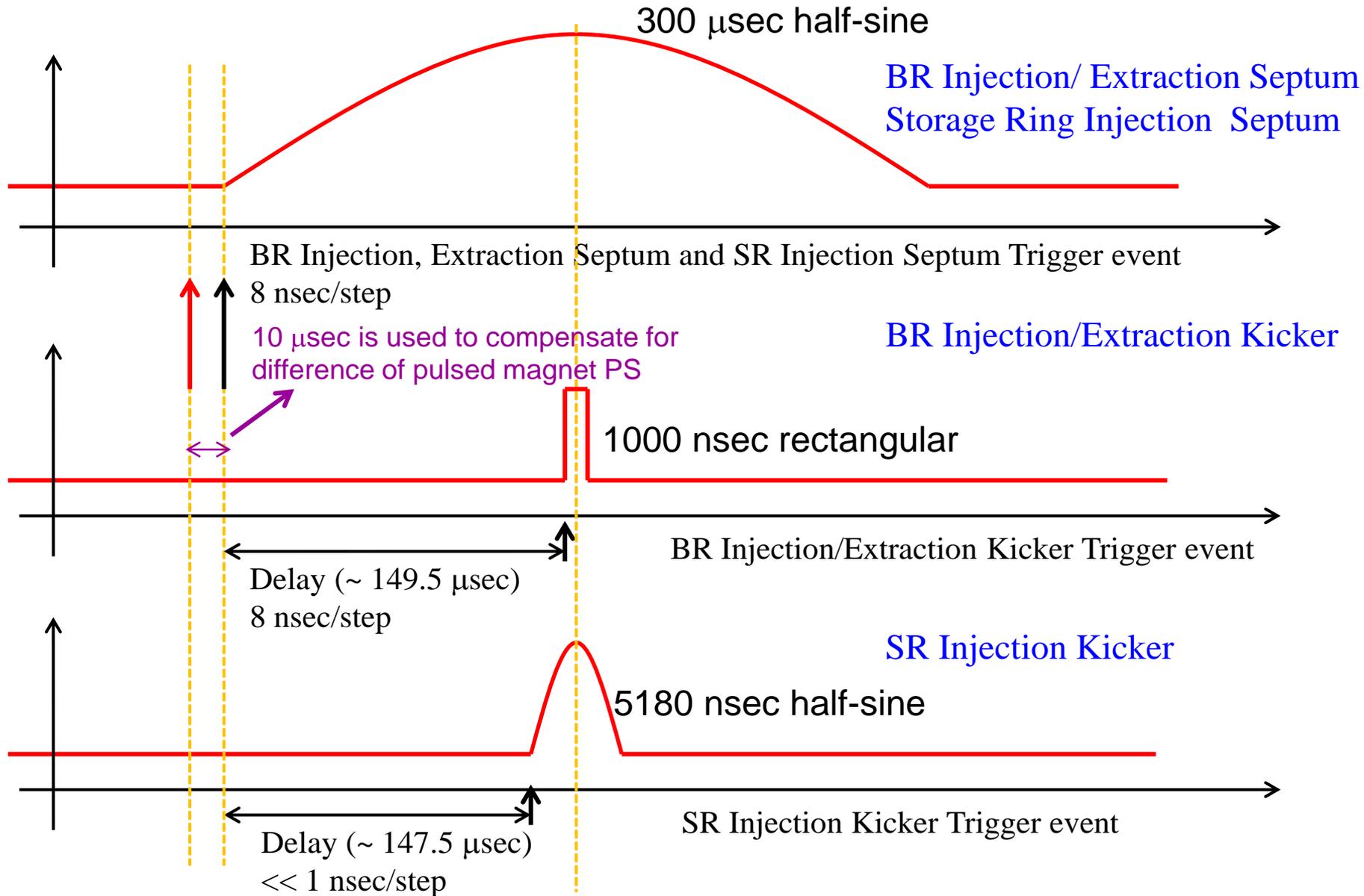


a. T-ZERO	at	0	μsec
b. BR-HW-TRIG	at	1	μsec
c. LINAC-PRE-INJ	at	10000	μsec
d. BR-PRE-INJ	at	10000 - 10	μsec
e. BR-PRE-EXTR	at	160000 - 5	μsec
f. SR-PRE-INJ	at	160000 - 5	μsec
g. SR-INJ	at	160000 - 5	μsec

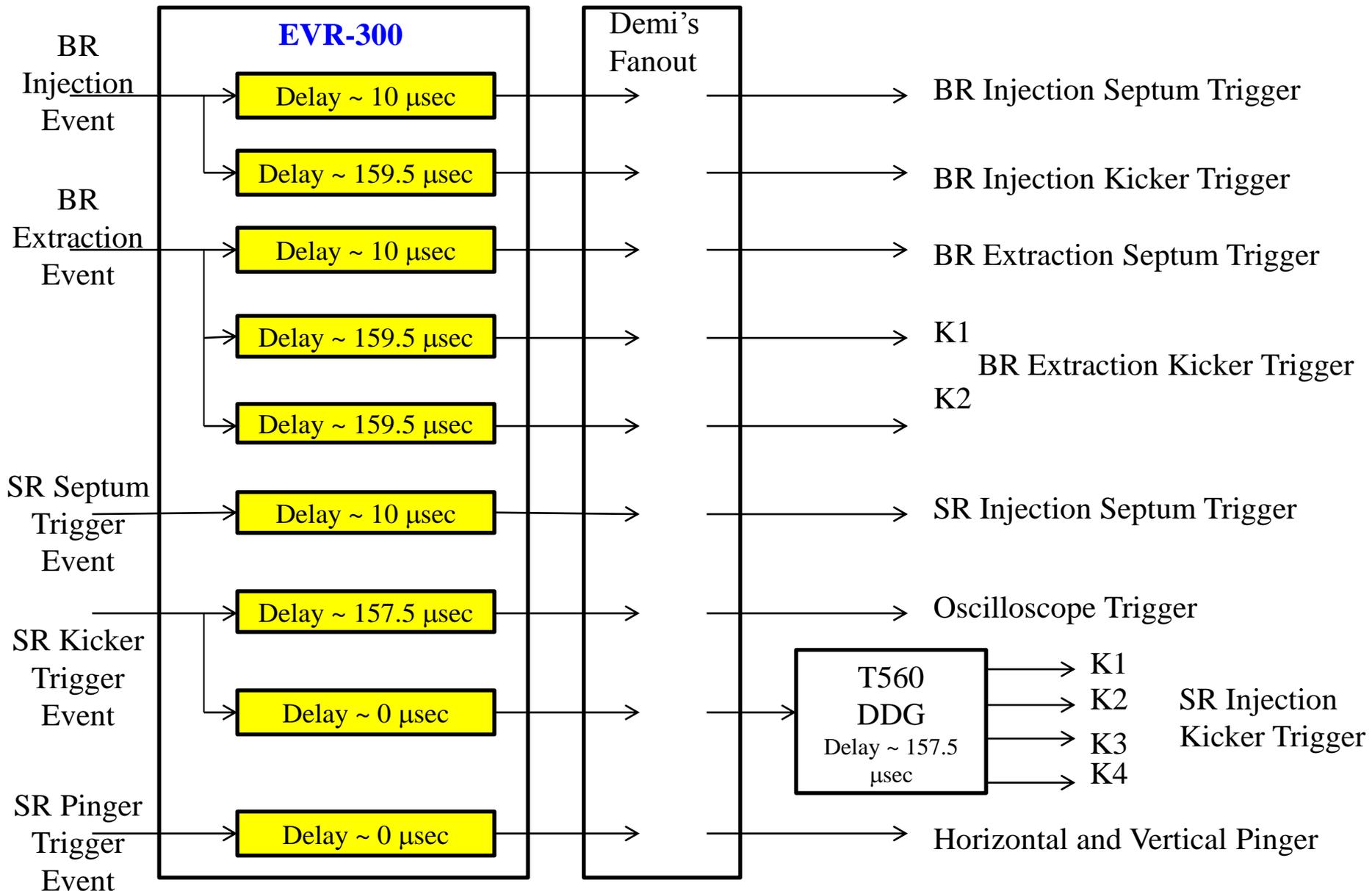
Booster Synchrotron Power Supply Waveform Plans



Pulsed Magnets Trigger Scheme



Pulsed Magnets Trigger Scheme - cont.



Sequence RAM of EVG

Sequence RAM of EVG : allows generation of well defined event sequence with precise relative delays

RAM address	32 bits Event address/time stamp	8 bits event code
0	Timestamp_0	Event_0
1	Timestamp_1	Event_1
2	Timestamp_2	Event_2
3		
...		
2047		

Sequence RAM - Individual Device Trigger Control

RAM Address	Delay Time	ON Every Shot		OFF		ON LINAC-PRE-INJ	
		Timestamp	Event Code	Timestamp	Event Code	Timestamp	Event Code
0	0 μ s	0000000	0x20	0000000	0x20	0000000	0x20
1	1 μ s	0000125	0x21	0000125	0x21	0000125	0x21
2	2 μ s	0000250	0x22	0000250	0x22	0000250	0x22
3	9990 μ s	1248750	0x23	1248750	0x23	1248750	0x23
4	10000 μ s	1250000	0x24	1250000	0x00	1250000	0x24
5	160000 μ s	20000000	0x25	20000000	0x25	20000000	0x25

n-1
N	170000 μ s	21250000	0x7f	21250000	0x7f	21250000	0x7f
n+1							
2047							

LINAC-PRE-INJ

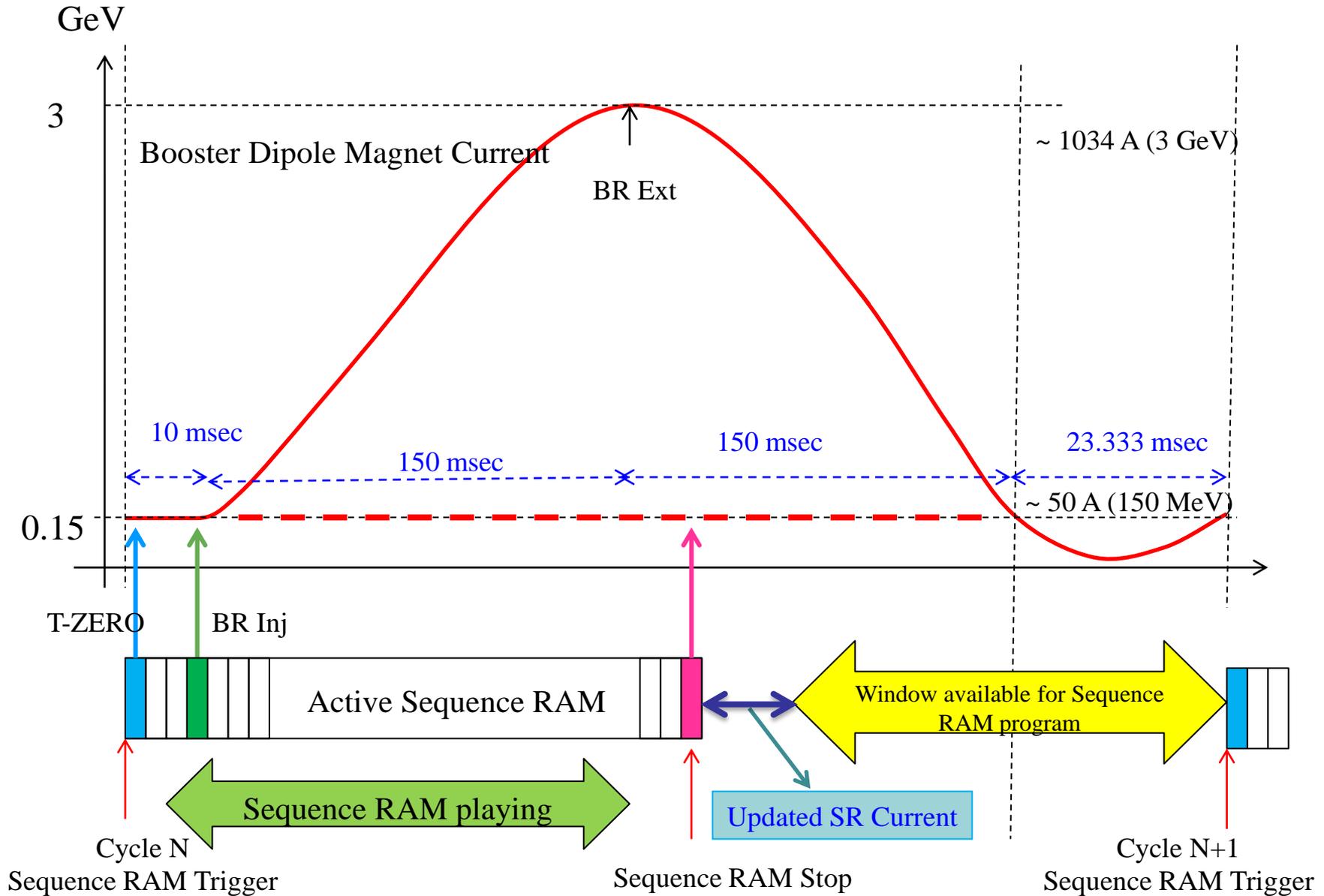


Null Event Code

Refresh on 3 Hz rate
If LINAC-PRE-INJ active
=> ON
If LINAC-PRE-INJ inactive
=> OFF

Stop Sequence RAM

Sequence RAM Programming at Every Cycle



Machine Cycle Definition following state

Linac Pre-injection

Linac RF ON

Booster Pre-injection

Linac RF ON

Booster Injection Septum ON

Booster Injection

Booster PS ON

Linac RF ON

Booster Injection Septum ON

Booster Injection Kicker ON

E-Gun ON

Booster Pre-extraction

Booster Extraction Septum ON

Booster Extraction

Booster Extraction Kicker ON

SR Pre-injection

SR Injection Septum ON

SR Injection

SR Injection Kickers ON

.....

Injection Modes

Beam Modes:

Single Bunch Mode (SB Mode)

Per Bunch Current

How many bunches (for multiple isolated bunches)

Bucket Address

Bucker address jump

Multi-Bunch Mode (MB Mode)

Current

Bunch train length

Bucket Address

Camshaft Mode

Combine SB and MB Mode

Top-up Mode

Support all above Mode (s)

Injection Control related EPICS IOCs

Timing Master IOC
(Include Injection Control)

Gun Timing,
Linac Timing,
Timing Diagnostic
Injection Control
IOC

Injection Command:
Modes
Cycle Time
... etc.

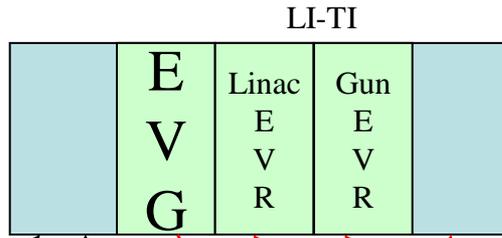
NPCT IOC
(Beam current,
Beam lifetime,
...)

Filling Pattern IOC
(Bunch current,
Bunch lifetime,
...)

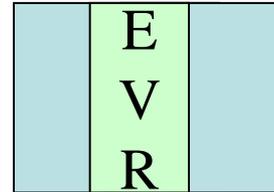
Desired Filling Pattern

Suggested next
bucket address
for injection

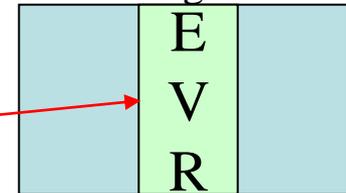
CA access



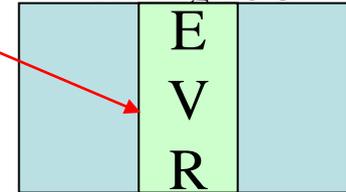
Timing
Backward Link
IOC



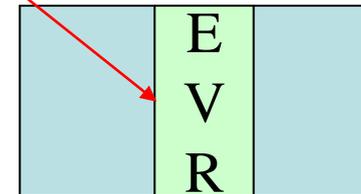
Booster Main PS
Timing IOC



Booster RF
Timing IOC

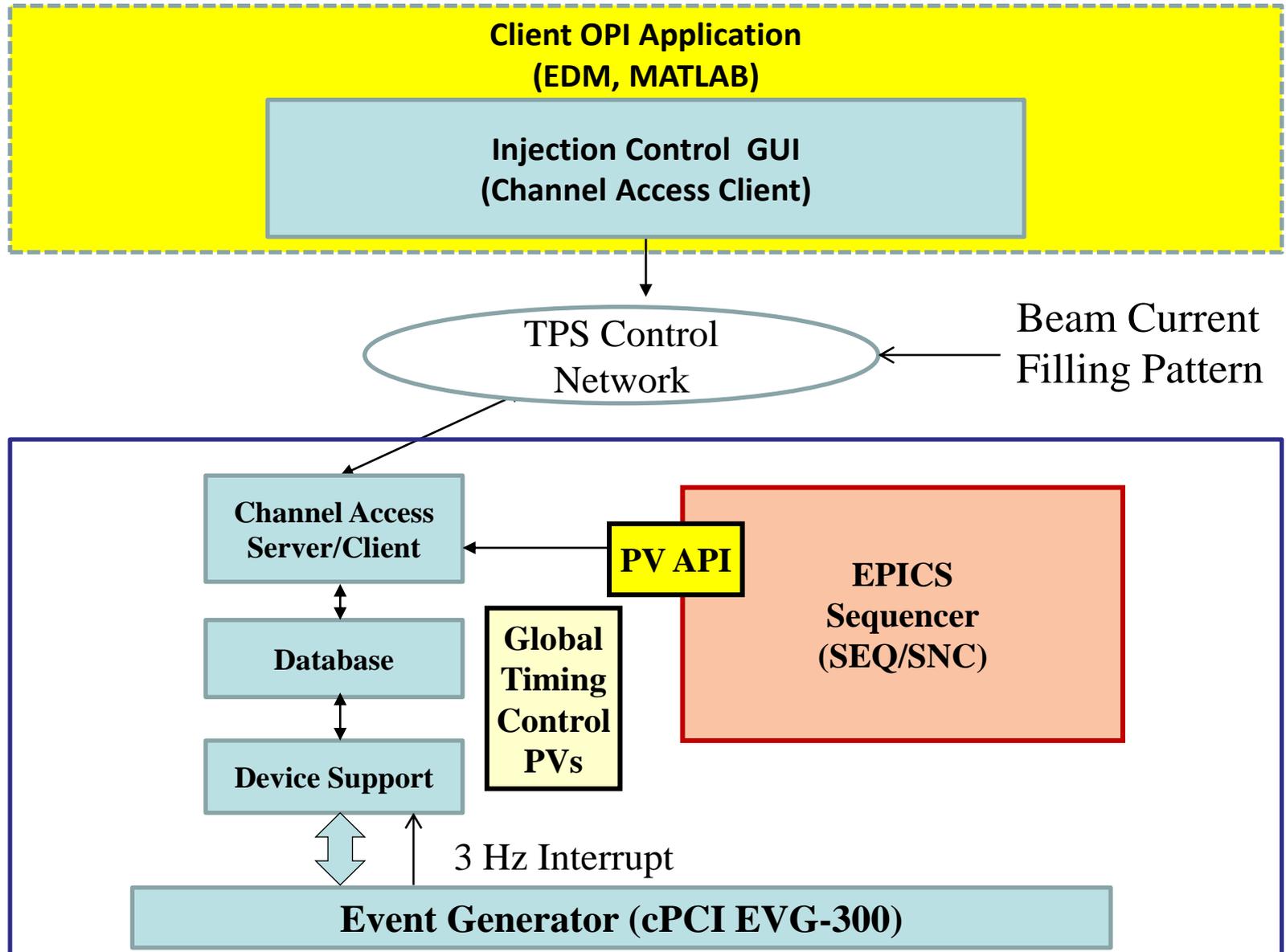


Injection and Extraction
Pulsed Magnets Power Supply
Timing IOC

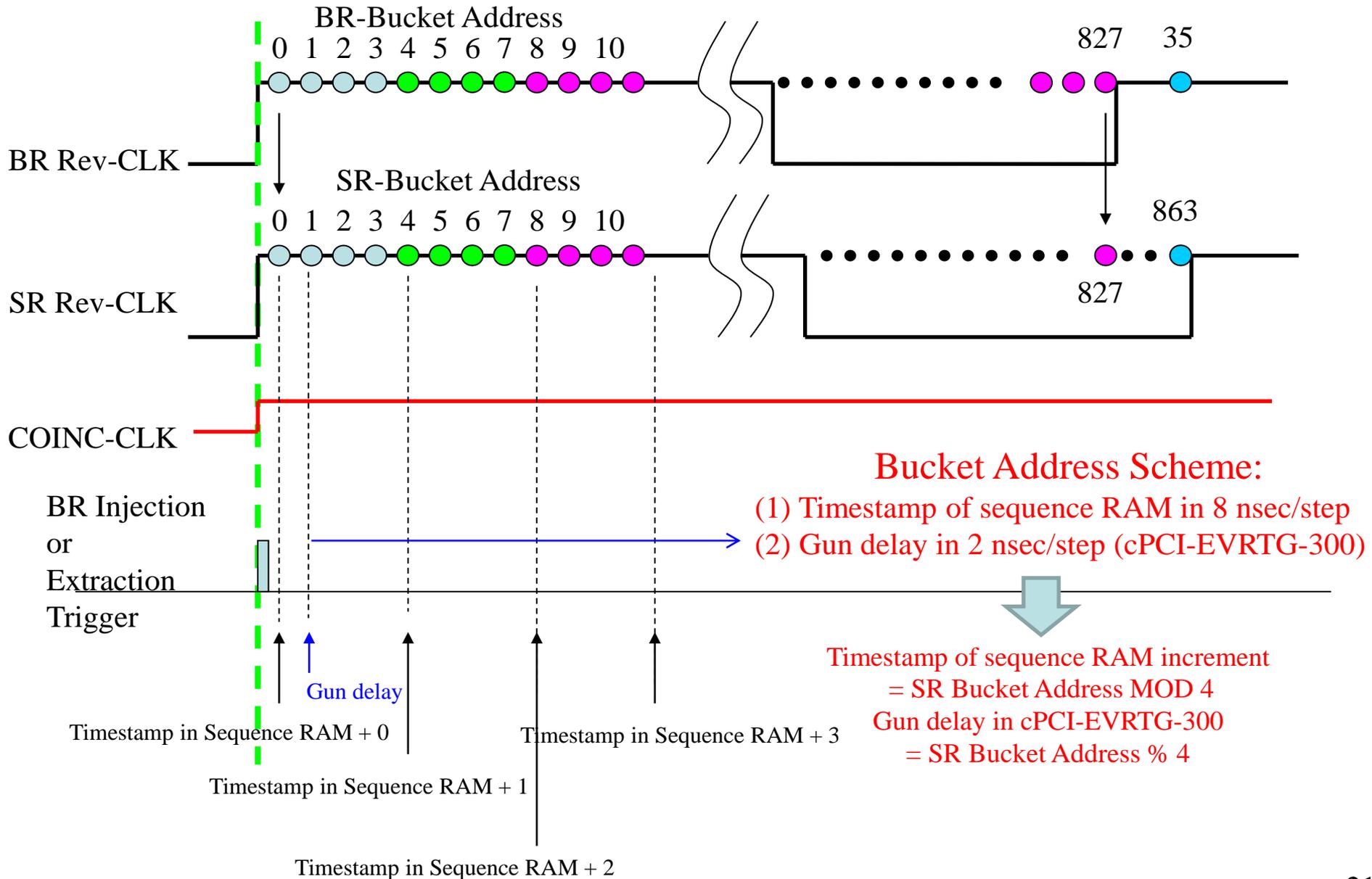


Timing Fanout

TPS Timing Sequencer Structure (SNL Option)



Issue on Bucket Addressing



Example of Bucket Addressing Process

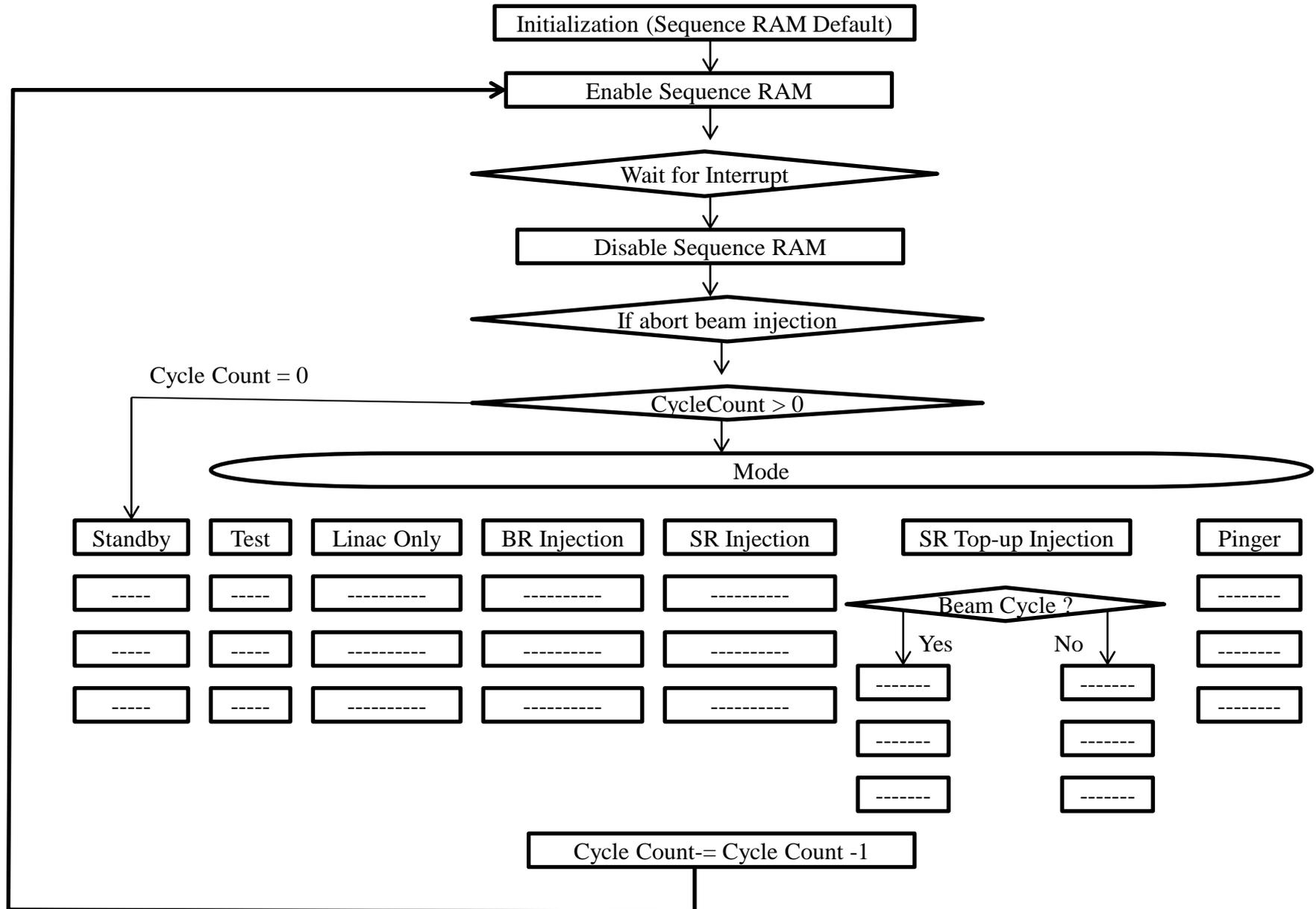
RAM Address	Delay Time	Bucket Address: 0		Bucket Address: 132		Bucket Address: 133		Bucket Address: 134	
		Timestamp	Event Code	Timestamp	Event Code	Timestamp	Event Code	Timestamp	Event Code
0	0 μ s	0000000	0x20	0000000	0x20	0000000	0x20	0000000	0x20
1	1 μ s	0000125	0x21	0000125	0x21	0000125	0x21	0000125	0x21
2	2 μ s	0000250	0x22	0000250	0x22	0000250	0x22	0000250	0x22
3	9990 μ s	1248750	0x23	1248783	0x23	1248783	0x23	1248783	0x23
4	10000 μ s	1250000	0x24	1250033	0x24	1250033	0x24	1250033	0x24
5	160000 μ s	20000000	0x25	20000033	0x25	20000033	0x25	20000033	0x25

n-1
n	170000 μ s	21250000	0x7f	21250000	0x7f	21250000	0x7f	21250000	0x7f
n+1									
2047									

Only change timestamp of injection beam related events

Timestamp increment	+ 0	+ 33	+ 33	+ 33
E-GUN Phase Shift (cPCI-EVRTG-300)	+ 0 nsec	+ 0 nsec	+ 2 nsec	+ 4 nsec

Functional Flowchart of the Timing Sequencer



Beamline and Experimental Station Timing Interface

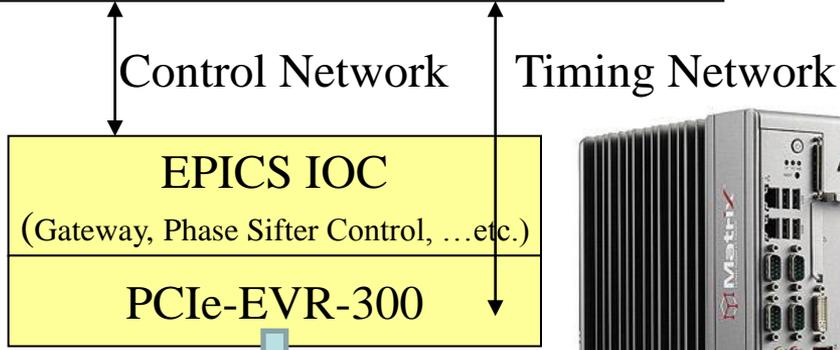
Standard Interface



Only available for users who need low jitter clock



PCIe-EVR-300
91.7 mm x 79.2 mm



Interface Board IFB-300



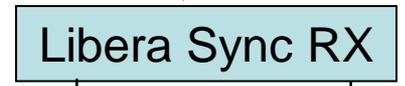
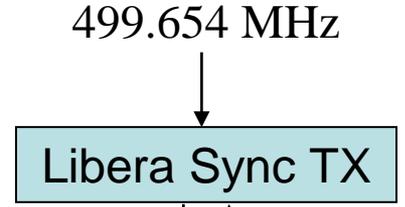
UNIV I/O 0
(TTL or NIM)
Short Gate

UNIV I/O 3
(TTL or NIM)
SR Clock

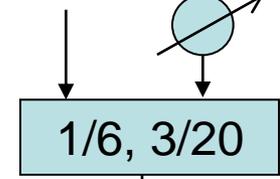
UNIV I/O 1
(TTL or NIM)
Long Gate

UNIV I/O 4
(TTL or NIM)
Injection

1 ~ 10 KHz
(Laser Amplifier)



ReSync

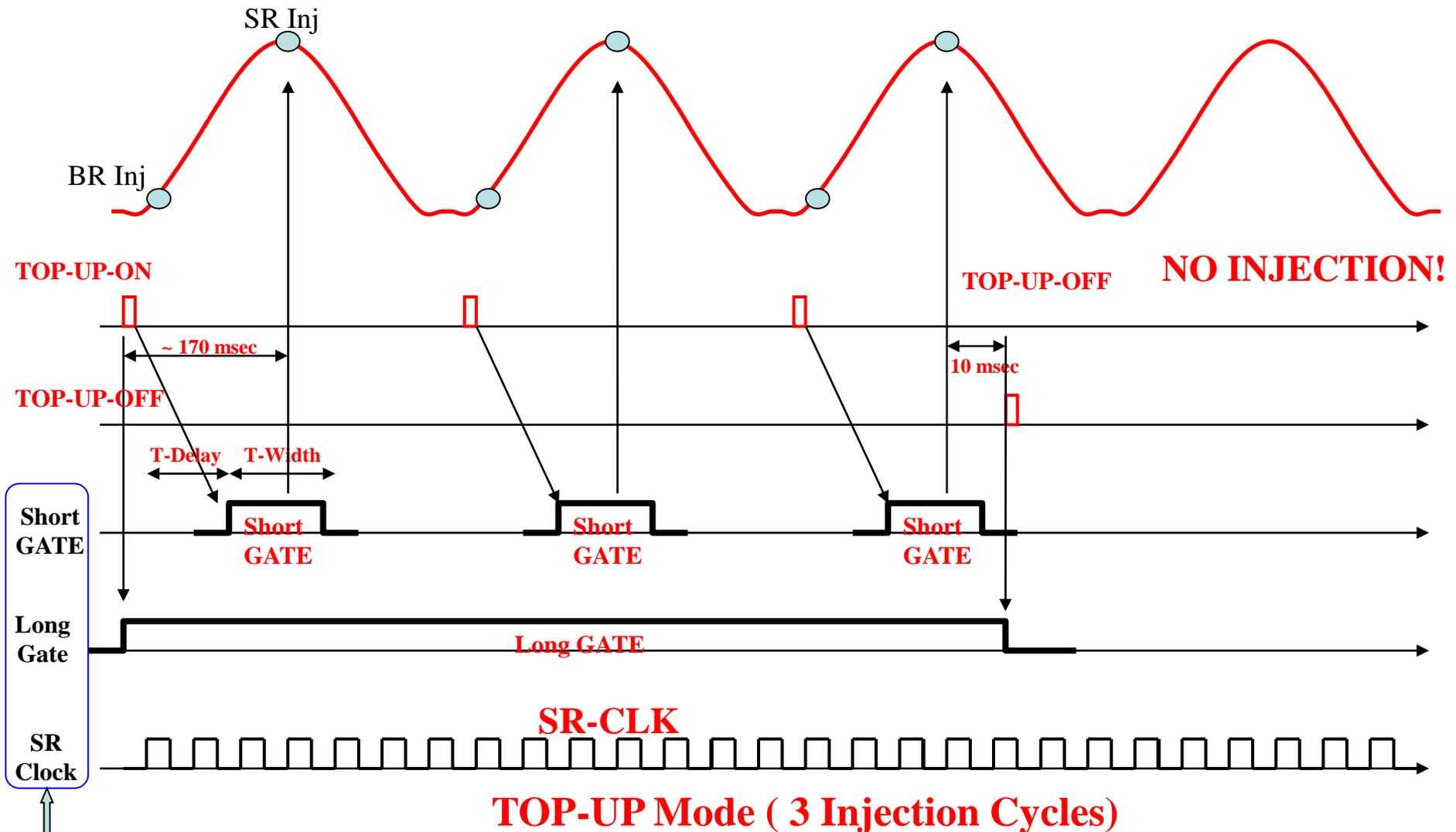


Phase Shifter
(I/Q type?)

83.2757 MHz
or
74.9481 MHz

499.654 MHz

Top-up Gating Timing Signals of Beamline



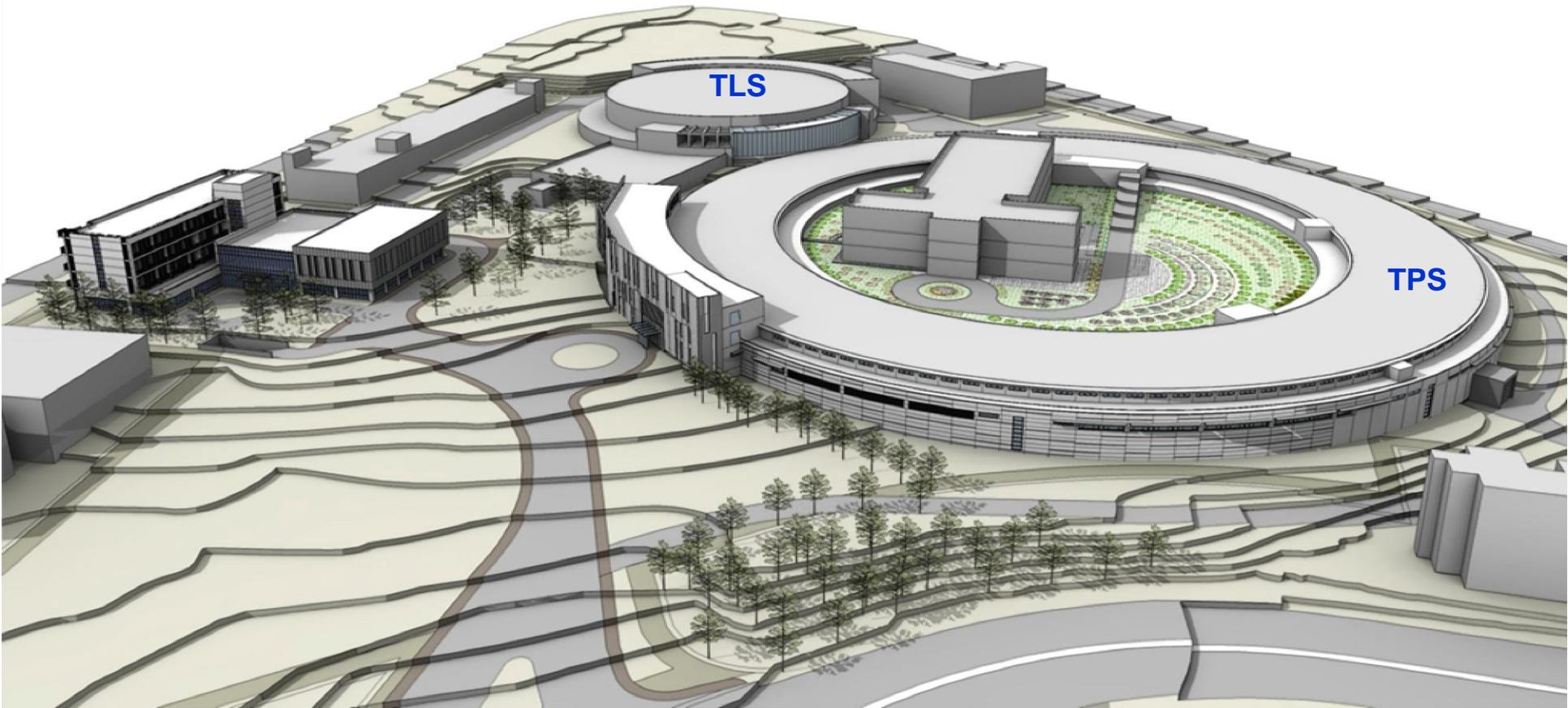
TOP-UP-OFF NO INJECTION!

TOP-UP Mode (3 Injection Cycles)

Timing Signals available for Beamlines

Summary

- The first lot of EVG/EVR/Fan-out concentrator modules was received in December 2010
- Setup test system has been started from February 2011
- Linac timing is ready for commissioning of the TPS linac in April 2011
- First prototyping of timing sequencer test by Matlab scripts was tested in 2011.
- Implementation of timing sequencer base on EPICS SNL is on-going.
- Installation of TPS timing system is scheduled in the 3rd quarter of 2013.
- Full scale Test of TPS timing system is scheduled in late 2013.



Thank You for Your Attention