

MRF Timing System IOC Status

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EPICS Collaboration Meeting Fall '11

Outline

Timing Background

Current Developments

In Depth

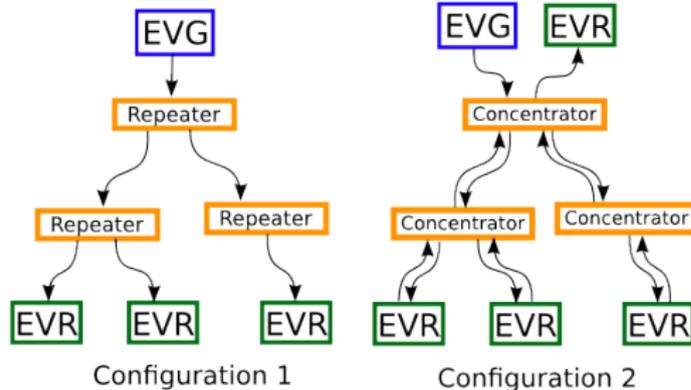
Terms

- ▶ Event
 - ▶ A point in time. Often defined in relation to another point.
- ▶ Code
 - ▶ An 8-bit number used to identify an event
- ▶ EVG
 - ▶ Event Generator - Broadcasts event codes
- ▶ EVR
 - ▶ Event Receiver - Decodes events and takes local actions
- ▶ MRF
 - ▶ Micro Research Finland Oy - <http://www.mrf.fi/>

Architecture

Components

- ▶ EVG
- ▶ EVR
- ▶ Repeater
 - ▶ Hub
- ▶ Concentrator
 - ▶ Switch



Synchronization

- ▶ Generator (EVG) accepts input from external RF clock (no PLL)
- ▶ 8b10 encoding (16-bit frame)
 - ▶ Event link bit rate 20x event code rate
 - ▶ $500 \text{ MHz RF} \div 4 = 125 \text{ MHz event} \times 20 = 2.5 \text{ GHz link}$
- ▶ 8-bit event code, 8-bit data (Distributed Bus)
- ▶ Each Receiver (EVR) has a PLL tuned $\pm 20 \text{ ppm}$ (10 kHz @ 500MHz)
- ▶ Dynamic tuning possible

Global Time Distribution

- ▶ Timestamp in two parts: seconds+counter
- ▶ Seconds distributed as 32-bit unsigned integer
- ▶ Counter driven by Event clock, Distributed Bus bit 2, or event code 0x7d
- ▶ One event code loads seconds and zeros counter
- ▶ Use PPS from GPS receiver

Use for NSLSII

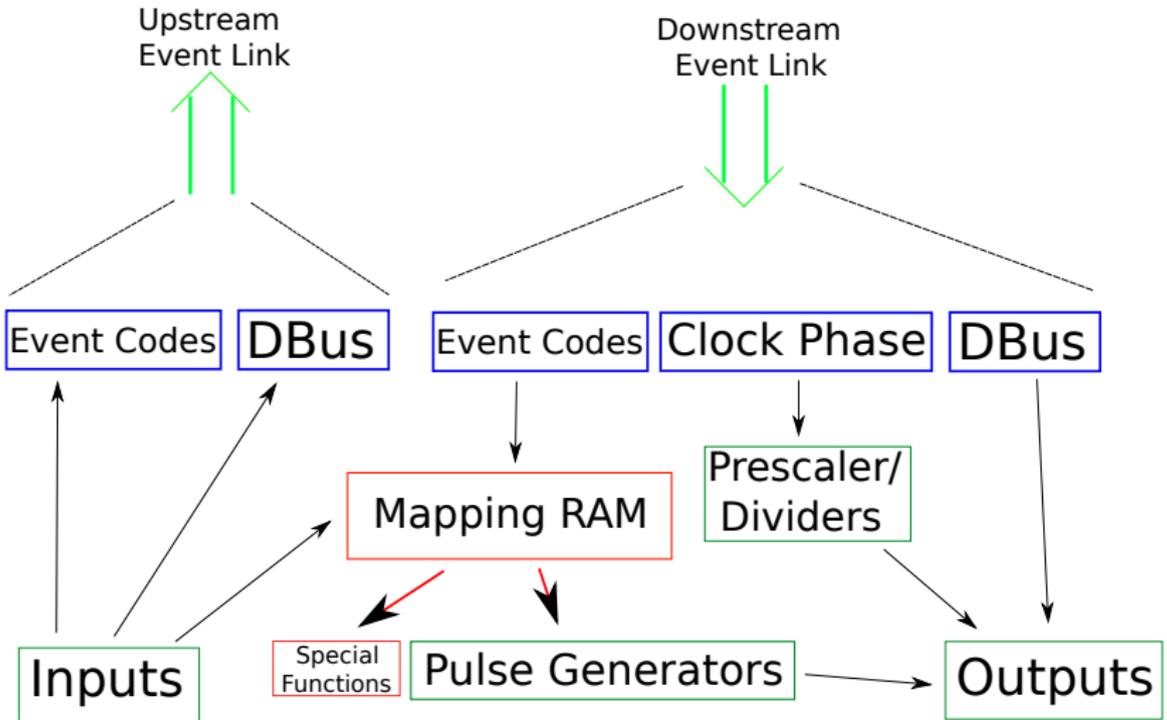
- ▶ EVG in main computer room with fanouts to all 30 cells, RF, and injector buildings.
- ▶ All pulls have same length.
- ▶ Each cell has additional local fanouts
- ▶ VME-EVRRF-230 is standard equipment.
 - ▶ TTL for general triggers
 - ▶ CML for special cases. Output fill pattern. Trigger kickers.
- ▶ cPCI-EVRTG-300 + GUNRC-300 to trigger electron gun.
- ▶ PMC-EVR-230 in some Linux servers (softloc hosts)
 - ▶ Use PMC to PCIe carrier board (transparent to software)
 - ▶ More precise timestamps
 - ▶ One local TTL input

- ▶ Features:
 - ▶ Only Base recordtypes
 - ▶ As dynamic as possible
 - ▶ PCI support via devLib2
- ▶ EVR
 - ▶ Dynamic mapping (Mapping RAM)
 - ▶ Data buffer Tx/Rx (Compatible with 1.x)
- ▶ EVG
 - ▶ Fully modifiable event sequence
 - ▶ Timestamp distribution w/o special hardware
- ▶ Documentation

Current Status

- ▶ EVR
 - ▶ Working with prerelease firmware
 - ▶ Tested with VME64x, cPCI, and PMC
- ▶ EVG
 - ▶ VME model working
 - ▶ cPCI model not supported (no access to hardware)
- ▶ Deployed at BNL for NSLSII teststands (LINAC, BPMs, and PS controllers)
- ▶ Version 2.0.0 released

Receiver Hardware



Receiver Hardware

- ▶ Programmable pulse generator
 - ▶ Triggered by event code(s)
- ▶ Phase locked frequency source (F_{evt}/i)
- ▶ Global timestamp receiver
 - ▶ Wall clock
 - ▶ Event code # received
 - ▶ Local input
- ▶ Local inputs create timestamps or send upstream
 - ▶ Available as: VME, cPCI, and PMC

EVR Mapping Ram

- ▶ Many-to-many mapping of event code to function
 - ▶ Trigger pulse generator
 - ▶ Reset prescalers
 - ▶ Timestamp functions
- ▶ Most cases 1-to-1 (code 17 triggers pulse gen. 4)
- ▶ Some are small-to-small
- ▶ Few are many-to-many (FIFO, Event log)

Mapping Records

- ▶ One record per pairing
- ▶ Default DB maps 3 events

```
record(longout , "pul4:trig1") {  
  field(DTYP, "EVR_Pulser_Mapping")  
  field(OUT, "@OBJ=EVR1:Pul0,Func=Trig")  
  field(VAL, "0x40")  
}
```

```
record(longout , "blk1") {  
  field(DTYP, "EVR_Mapping")  
  field(OUT, "@OBJ=EVR1,Func=Blink")  
  field(VAL, "0x40")  
}
```

Data Buffer

- ▶ Buffer reception in two stage. High priority thread reads from hardware places in FIFO. Lower priority thread takes from FIFO and runs callback list.
- ▶ Waveform device support to receive. Does endian conversion for multibyte types.
- ▶ Plan to use this to distribute fill pattern for NSLSII.

Event FIFO Buffer

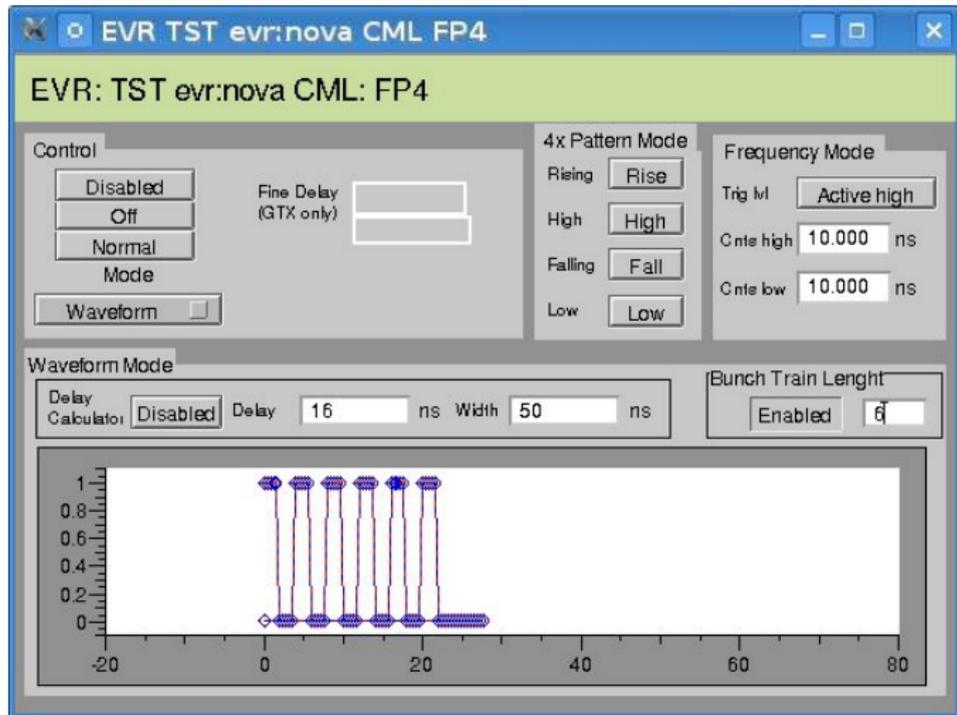
- ▶ Arrival of an “interesting” event is recorded in a hardware FIFO buffer.
- ▶ I/O Intr scan and callback list.
- ▶ longin device support to process on event reception.
- ▶ Throttling to prevent too fast events from taking 100% of CPU. Limit buffered events to a given rate. Also, do not run callback list until all previous processing is complete.

Timestamp Validation

- ▶ Must prevent invalid timestamps from propogating into `generalTime`.
- ▶ Several times a misconfiguration caused one second tick to be sent too often, or out of sync.
- ▶ Firmware bug (now fixed) caused occasional invalid reads.
- ▶ EVR must receive 5 sequential updates before it will start using time. Invalid if out of order time is received.

CML/GTX Pattern Outputs

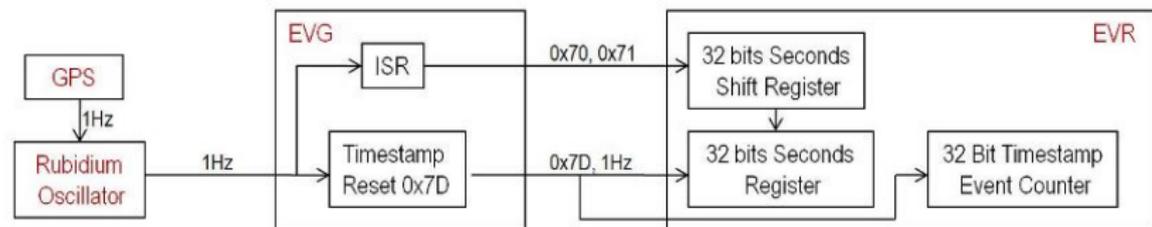
- ▶ Higher resolution. 20x EVRRF, 40x EVRTG (effective 8x)
- ▶ Output multi-bit patterns



Generator Hardware

- ▶ Send periodic event and/or data
- ▶ Send event sequences
 - ▶ Preset list of times and codes (eg. linac shot or booster ramp)
- ▶ Currently VME only, in future cPCI only.

Timestamp



- ▶ Synchronize to GPS without custom electronics.
- ▶ Off the shelf GPS receiver with NTP server and 1Hz TTL output.
- ▶ Buffered with Rubidium oscillator for high precision. Continues running if GPS 1Hz is lost.
- ▶ 1Hz send special event code and interrupts CPU
 - ▶ Special event code 0x7D marks start of a second (hardware only)
 - ▶ Interrupt sends next second bit by bit. POSIX time by default.

EVG Sequences

- ▶ Example. Timeline for injection/top off
 - ▶ Start insertion kicker ramp up
 - ▶ wait 100us
 - ▶ Trigger Klystron modulators
 - ▶ wait 20us
 - ▶ Trigger Klystron
 - ▶ wait 500ns
 - ▶ trigger e^- gun
 - ▶ wait 10us
 - ▶ Start insertion kicker ramp down

Delay	Code
0	0x10
12500	0x20
2500	0x25
61	0x40
1250	0x12

Note: This is how it looks in hardware

Sequence Use Cases

- ▶ NSLSII Booster is $\frac{1}{5}$ diameter or Storage ring.
- ▶ Filling/top off process involves multiple injections
- ▶ Need to control how many bunches and where they go
- ▶ Use timing system to select which sector to fill
 - ▶ “Fill Manager” process sets booster extraction delay
 - ▶ Move ≥ 1 events
- ▶ Allow programmatic manipulation w/o complicating client(s)

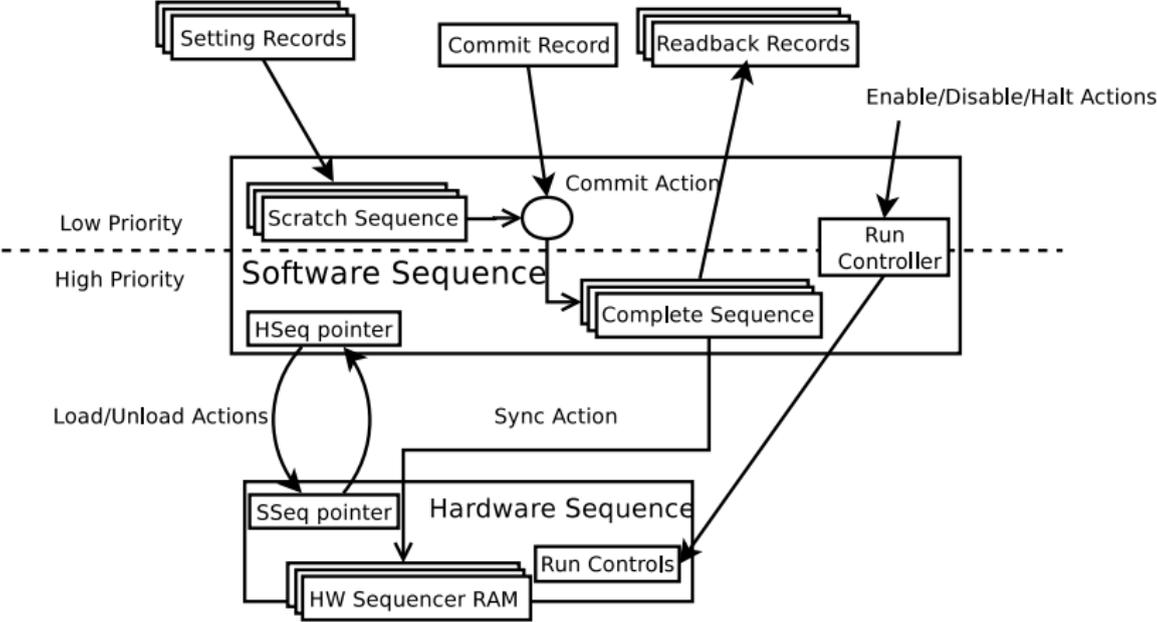
Sequence Representation

- ▶ 2 waveforms (codes and times)
 - ▶ Clients have to know array index
 - ▶ Ordering
- ▶ Trigger source/mode
- ▶ Control (commit, (un)load, enable/disable)

Sequence Management

- ▶ Manage user interactions with sequence ram
- ▶ Current hardware supports two independent sequences.
- ▶ Single shot or repeating
- ▶ Don't modify while running

Model



Sequencer Workflow

1. Modify scratch sequence

- ▶ DB/CA operations of individual records (synchronous device supports)
- ▶ CA put w/ callback

2. Commit

- ▶ Single DB/CA operation
- ▶ Updates complete sequence

3. Sync

- ▶ When loaded, or at end of run if already loaded
- ▶ Automatic

Interface

Event Code / Timestamp

Run Mode

Normal

Normal

Timestamp Input

EGU

mSec

Trigger Source

Mxc0

Mxc0

Committed

Commit

Loaded

Load Unload Trigger

Enabled

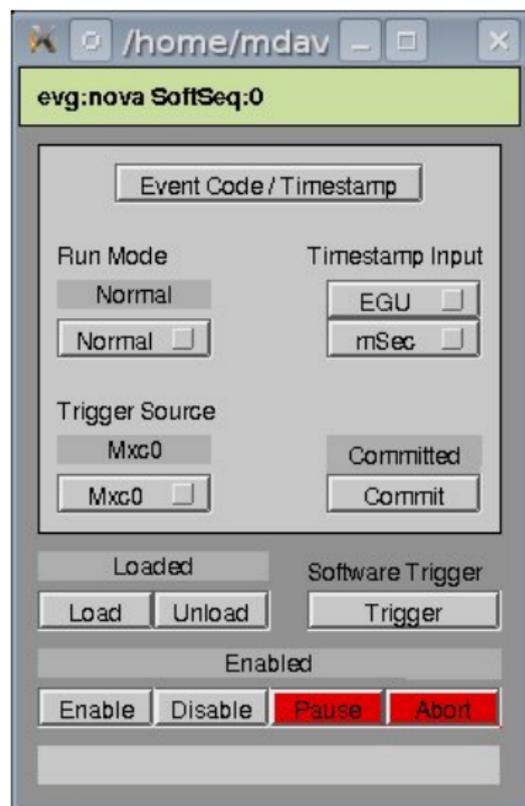
Enable Disable **Pause** **Abort**

evg:nova SoftSeq:0

	Event Code	Timestamp
1	10	0
2	11	10
3	12	500
4	11	510
5		
6		
7		

Set

Sequence Control



- ▶ Run Mode
 - ▶ **Single**
 - ▶ Disarm after one run
 - ▶ **Normal**
 - ▶ rearm after each run
 - ▶ **Automatic**
 - ▶ continuous run
- ▶ Trigger Source
 - ▶ For Single and Normal
- ▶ Units
 - ▶ Meaning of time delay
- ▶ Commit
 - ▶ Propagate changes to hardware

Sequence Control (2)

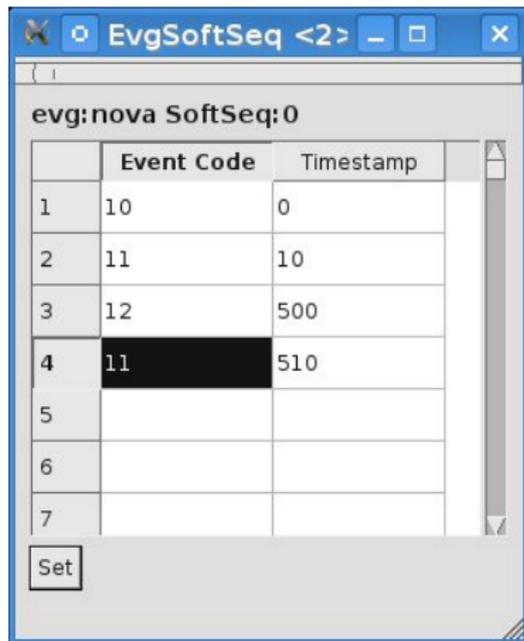


- ▶ Load/Unload
 - ▶ (De)Allocate hardware resources to run this sequence
- ▶ Enabled
 - ▶ Trigger permit
- ▶ Disable
 - ▶ Prevent further triggers. If already triggered, run to completion
- ▶ Pause
 - ▶ Stop running sequence w/o reset.
- ▶ Abort
 - ▶ Immediately halt

Interface

Specify sequence. Units of Timestamp defined for each sequence.

Note: Pictured is a small PyQt+cothreads script to allow editing sequence waveforms in a table.



The screenshot shows a window titled "EvgSoftSeq <2>". Inside the window, the text "evg:nova SoftSeq:0" is displayed above a table. The table has two columns: "Event Code" and "Timestamp". The rows are numbered 1 through 7. Row 4 is highlighted in black. Below the table is a "Set" button.

	Event Code	Timestamp
1	10	0
2	11	10
3	12	500
4	11	510
5		
6		
7		

Demo

Attempt to run live demo.