

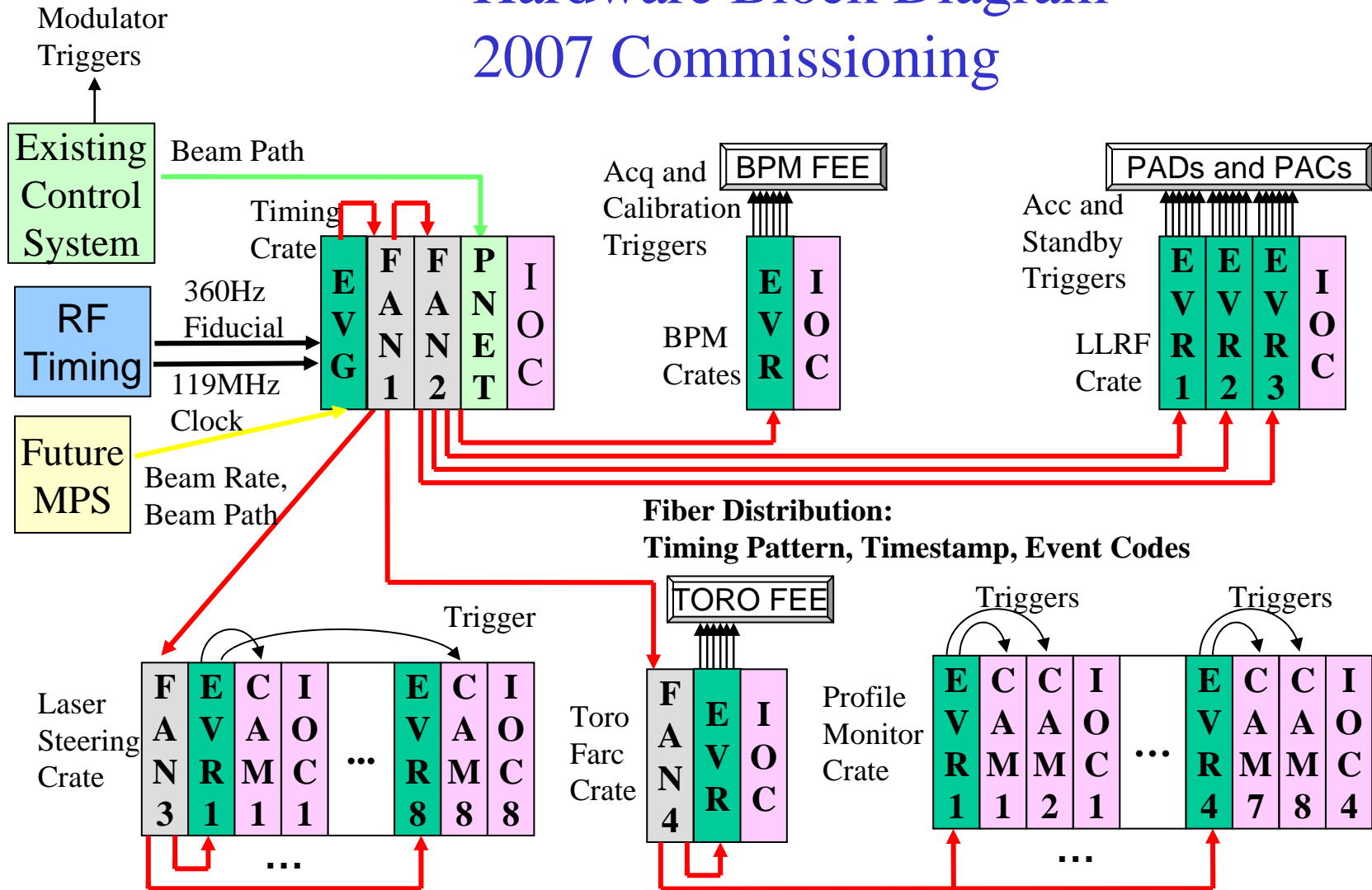
Timing and Event System

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Outline

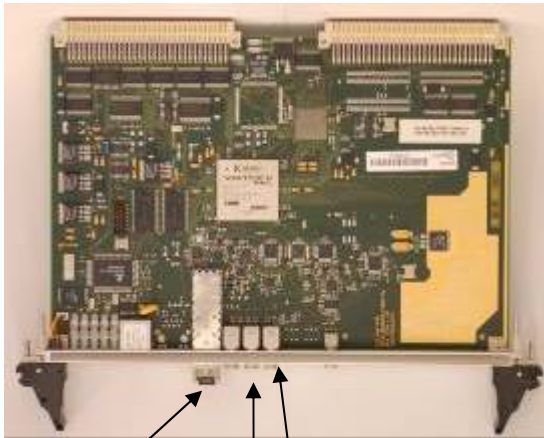
- Overview – HW and Reqts
- Hardware Test Stand
- Long-Haul Fiber Issues and Plans
- Outstanding Software Issues and Tasks
- Wish List

Hardware Block Diagram 2007 Commissioning



Micro-Research Finland Oy

Event Generator (EVG-200)



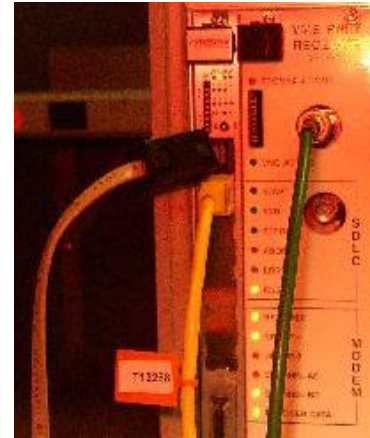
SFP transceiver
• Optical signal to EVRs (fan-outs)

RF input
• Event clock
• divided from RF
• /1*, /4, ... /12

Line synchronisation input
360 Hz

*SLAC addition

SLAC PNET Receiver



■ Receives the MPG broadcast sent to SLC micros and passes it to the EVG



EVR Fan Out module

Micro-Research Finland Oy

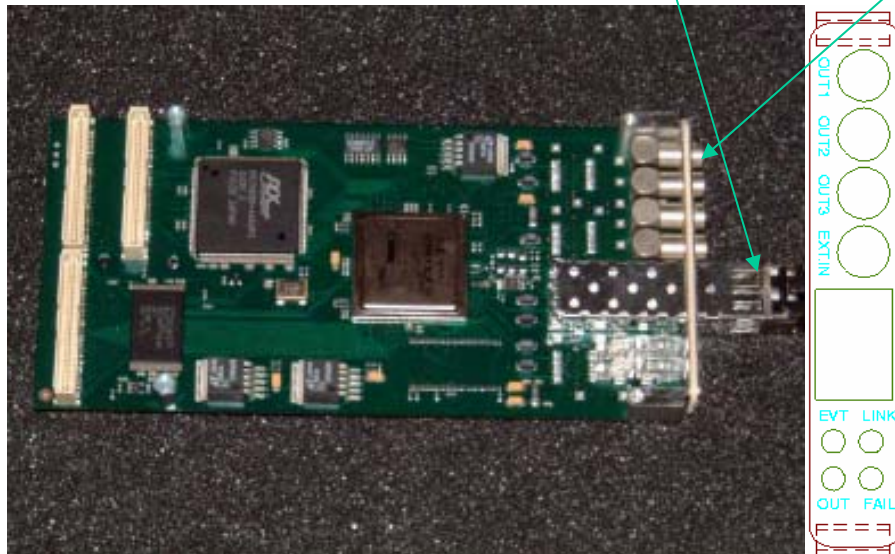
SFP transceiver
• Optical signal from EVG (or fan-out)

Programmable outputs

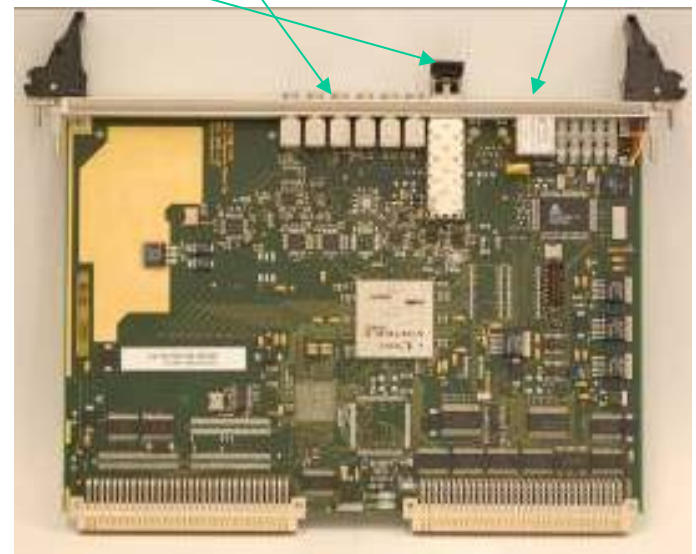
- 5(3) TTL level
- 2 LVPECL level

External trigger input

Recovered RF output



Event Receiver – PMC version



Event Receiver (EVR-200-RF)

Modifications to EVG

■ 119MHz clock input

- In the absence of a $\div 1$ input, a daughterboard was made containing a clock receiver IC to allow us to input 119MHz directly

■ EVG AC-line input

- 360Hz fiducial input was rerouted with firmware change to avoid addition of jitter from internal 10 kHz clock and phase shifter

Tallies for 2007, Plans for Next Phase

- # EVRs = 31 installed (mostly **PMC**)
 - Add 60 more EVRs - 34 VME, 26 PMC
- # IOCs with EVRs = 28
 - Add 40 more IOCs with EVRs
- # EVR **Fanouts** = 4
 - Add 5 more fanouts (1 every 200m)
- # Hardware Triggers = 120+
 - All TTL except 2 NIM triggers for QDCs
 - Most require short cables (except LLRF)
 - Add ? more

Timing Requirements

Maximum trigger rate	360 Hz
Clock frequency	119 MHz
Clock precision	20 ps
Coarse step size	8.4 ns \pm 20 ps
Delay range	>1 sec
Fine step size	20 ps
Max timing jitter w.r.t. clock	2 ps rms
Differential error, location to location	8 ns
Long term stability	20 ps

Event System Requirements

■ Event Generator IOC:

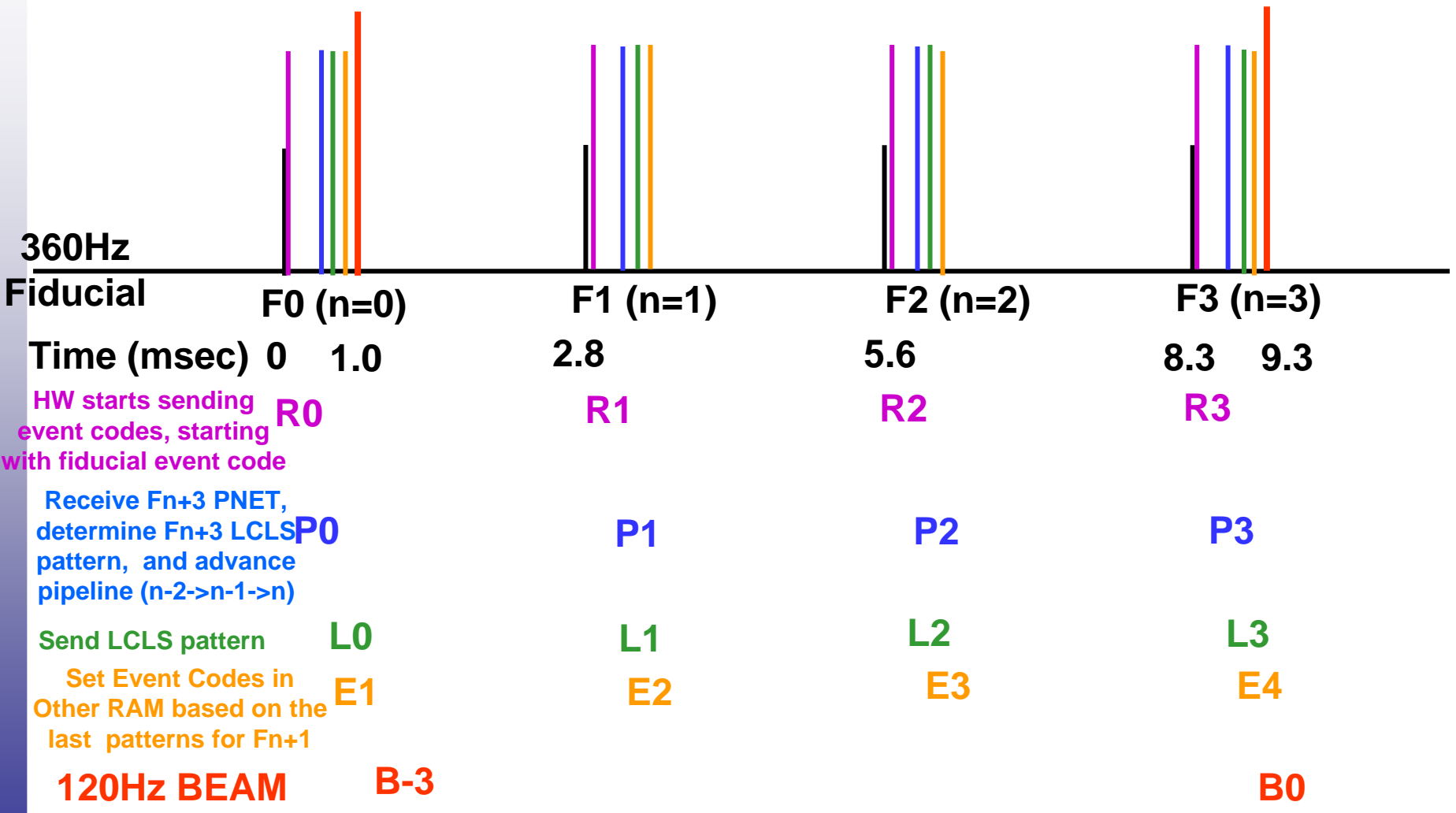
- Send out proper event codes at 360Hz based on:
 - PNET pattern input (beam code and bits that define beam path and other conditions)
 - Add LCLS conditions such as BPM calibration on off-beam pulses , diagnostic pulse etc.
- Future – event codes also based on new MPS and user input
- Send out system timestamp with encoded pulse ID from PNET
- Send out PNET pattern to be used by SLC-aware IOCs
- Manage user-defined beam-synchronous acquisition measurement definitions (event definition or EDEF)
- Check for match between user EDEFs and input PNET pattern at 360Hz and tag matches in outgoing pattern

Event System Requirements, cont

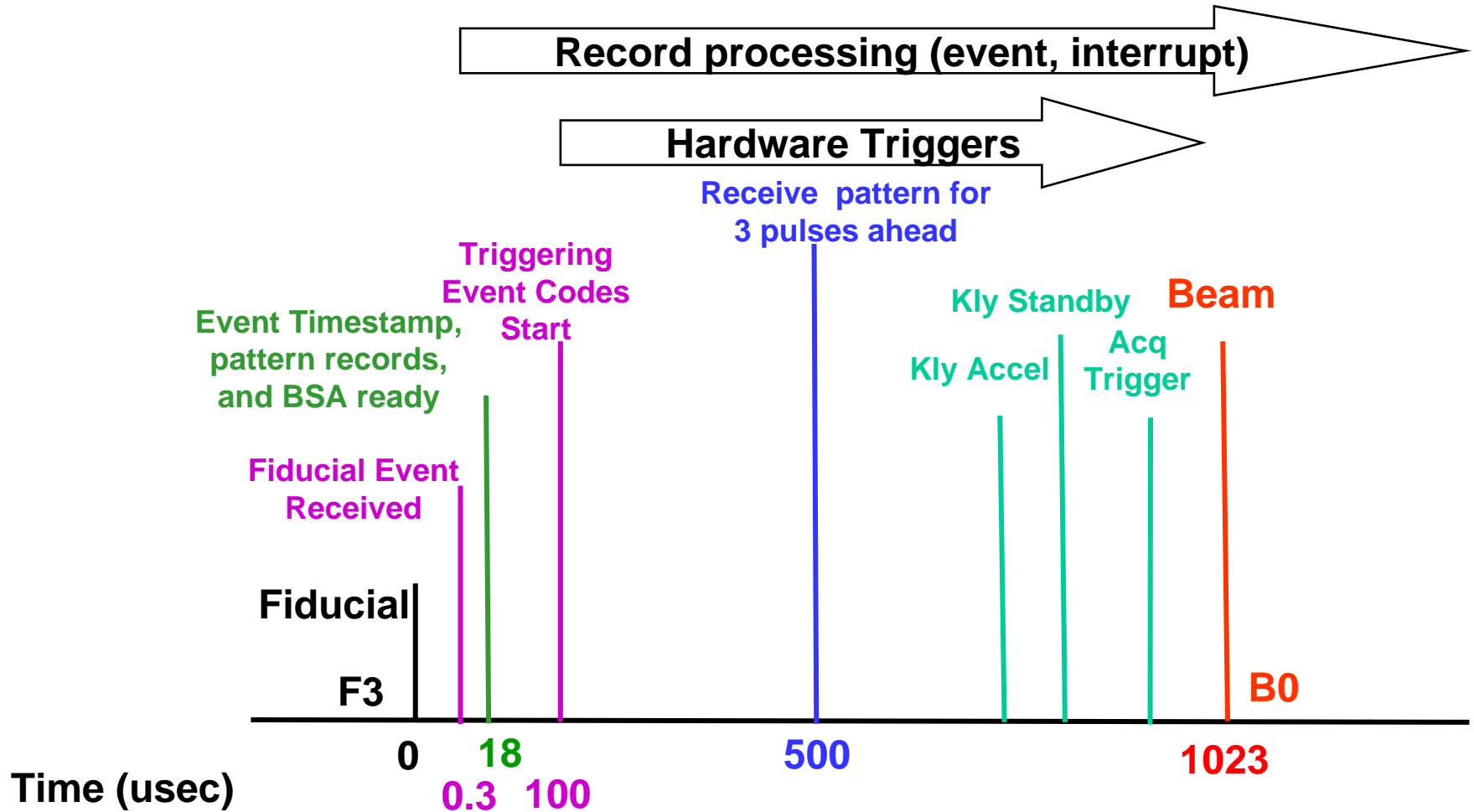
■ Event Receiver IOC:

- Set trigger delays, pulse widths, and enable/disable via user requests (not yet done on a pulse-by-pulse basis)
- Set event code per trigger (triggering done in HW when event code received)
- Receive event pattern 8.3 msec before corresponding pulse
- Perform beam-synchronous acquisition based on tags set by EVG in the event pattern
- Perform beam-synchronous acquisition for the SLC-aware IOC based on the PNET part of the event pattern
- Process pre-defined records when specific event codes are received (not yet available – bug!)

EVG Event Time Line – 4 Fiducials



Trigger Event Time Line – 1 Beam Pulse (B0)



Trigger Control Display

IN20-LI21 Events / Triggers - IN20 Stripline BPMs 2-G1

All TREFs...

Exit

Description	Diag	Polarity	Width(ns)	TDES(ns)*	TCTL	EVR Diags	* w.r. to TREF	
							Trig	Ch
BPM2		Inverted	100	750	Enabled	EVR:IN20:BP01...	TTB	0
BPM3		Inverted	100	800	Enabled	EVR:IN20:BP01...	TTB	1
BPM5		Inverted	100	750	Enabled	EVR:IN20:BP01...	TTB	2
BPM6		Inverted	100	800	Enabled	EVR:IN20:BP01...	TTB	3
BPM8		Inverted	100	800	Enabled	EVR:IN20:BP01...	TTB	4
BPMG1		Inverted	100	800	Enabled	EVR:IN20:BP01...	TTB	5
Spare		Normal	100	10	Enabled	EVR:IN20:BP01...	TTB	6
BPM2 Calibration		Normal	100	3900	Enabled	EVR:IN20:BP01...	TTB	7
BPM3 Calibration		Normal	100	3900	Enabled	EVR:IN20:BP01...	TTB	8
BPM5 Calibration		Normal	100	4000	Enabled	EVR:IN20:BP01...	TTB	9
BPM6 Calibration		Normal	100	4000	Enabled	EVR:IN20:BP01...	TTB	10
BPM8 Calibration		Normal	100	4000	Enabled	EVR:IN20:BP01...	TTB	11
BPMG1 Calibration		Normal	100	3950	Enabled	EVR:IN20:BP01...	TTB	12
Spare		Normal	100	10	Enabled	EVR:IN20:BP01...	TTB	13
Spare trigger 1		Normal	100	10	Enabled	EVR:IN20:BP01...	FP	0
Spare trigger 2		Normal	100	10	Enabled	EVR:IN20:BP01...	FP	1
Spare trigger 3		Normal	100	10	Enabled	EVR:IN20:BP01...	FP	2
Spare trigger 4		Normal	100	10	Enabled	EVR:IN20:BP01...	FP	3

Stripline BPMs 9-15...

Stripline BPMs S1-S3...

LI21 Stripline BPMs A11-M14...

Toro/FC/BLen...

EVG Displays

IN20 EVG Events Development

EXIT

Name	Event Code	Delay (Clock Ticks)	Delay (nsec)	Enable	Every Cycle
Fiducial	1	0	0		1
Heartbeat	122	1	1		1
360Hz	9	12950	108824	1	1
Modulo 36*	201	13000	109244	1	1

* Event codes cycle between 201 to 236.

Time Slot 1 to 6 Event Codes

LCLS Beam Events						Beam Code	Mask Setup
Beam Full	140	11900	100000	1	0	1	Masks
Beam&60Hz	141	11901	100008	1	0		
Beam&30Hz	142	11902	100017	1	0		
Beam&10Hz	143	11903	100025	1	0		
Beam & 5Hz	144	11904	100034	1	0		
Beam & 1Hz	145	11905	100042	1	0		
Beam&0.5Hz	146	11906	100050	1	0		
Full N-1	147	11907	100059	1	0	1	Masks
Full N-2	148	11908	100067	1	0	1	Masks
Beam TBD1	149	11909	100076	0	0	1	Masks
Burst	150	11910	100084	0	0	1	Masks
Klys Accel	151	11911	100093	1	0	1	Masks
Beam TBD2	152	11912	100101	0	0	1	Masks
RF Only	153	11913	100109	1	0	1	Masks
Beam TBD4	154	11914	100118	0	0	1	Masks
Straight Ahead Beam	155	11915	100126	1	0	3	Masks
Beam TBD6	157	11916	100135	0	0	1	Masks
Beam TBD7	158	11917	100143	0	0	1	Masks

IOC:IN20:EV01 EVG Diags Production

EXIT

	Pattern Pipeline			OK
	P-3	P-2	P-1	P0 (Now)
PULSEID	0x2D0	0x2CF	0x2CE	0x2CD
BEAMCD	9	0	18	0
TIMESLOT	1	6	5	4
MOD 1	0x8900	0x0	0x1200	0x0
MOD 2	0x6600001	0x20	0x10	0x6000008
MOD 3	0x1000000	0x0	0x0	0x0
MOD 4	0x20013FF0	0x80000000	0x80000000	0x80000000
MOD 5	0x1F00000	0x0	0x0	0x0
BUNCHG	0	0	0	0
AVGDONE	0xF7FDF	0xF7FDF	0xF7FDF	0xF7FDF

General Time

Time Pipeline

Seconds	0x208189D4	0x208189D4	0x208189D4	0x208189D4
Nsecs	0x299802D0	0x296C02CF	0x294202CE	0x291802CD
Status	0x0	0x0	0x0	0x0

Counters

All Counter Reset

MP00 PNET Bits

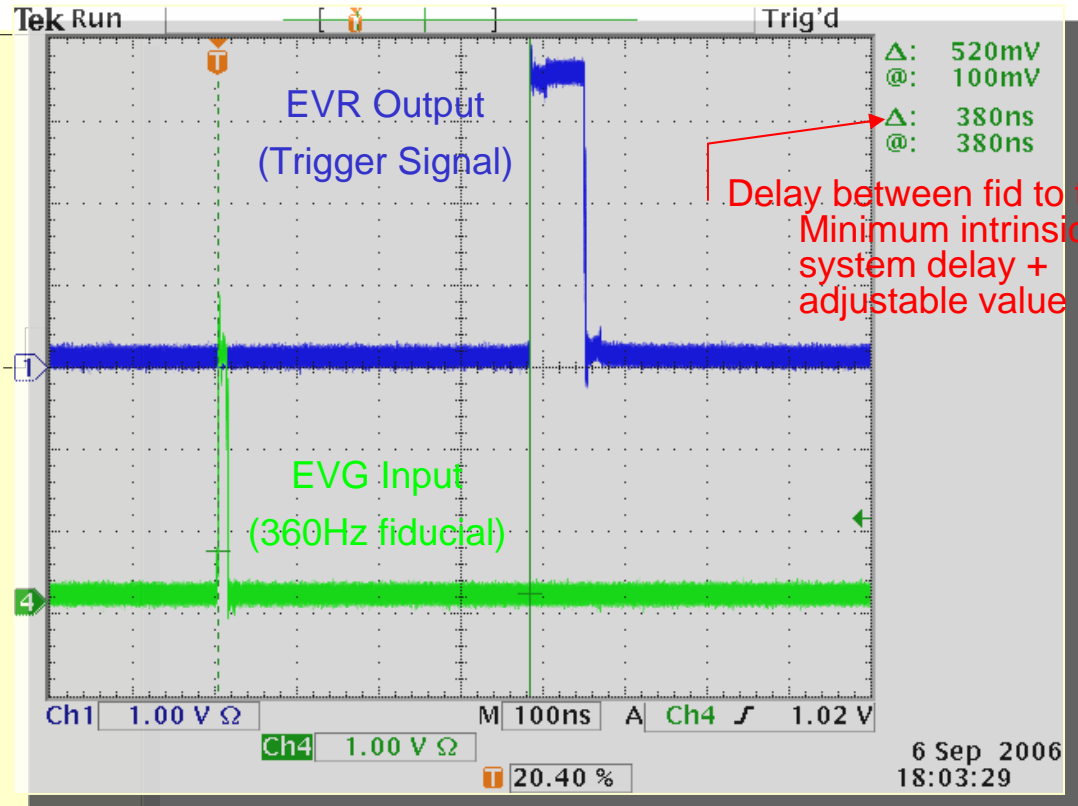
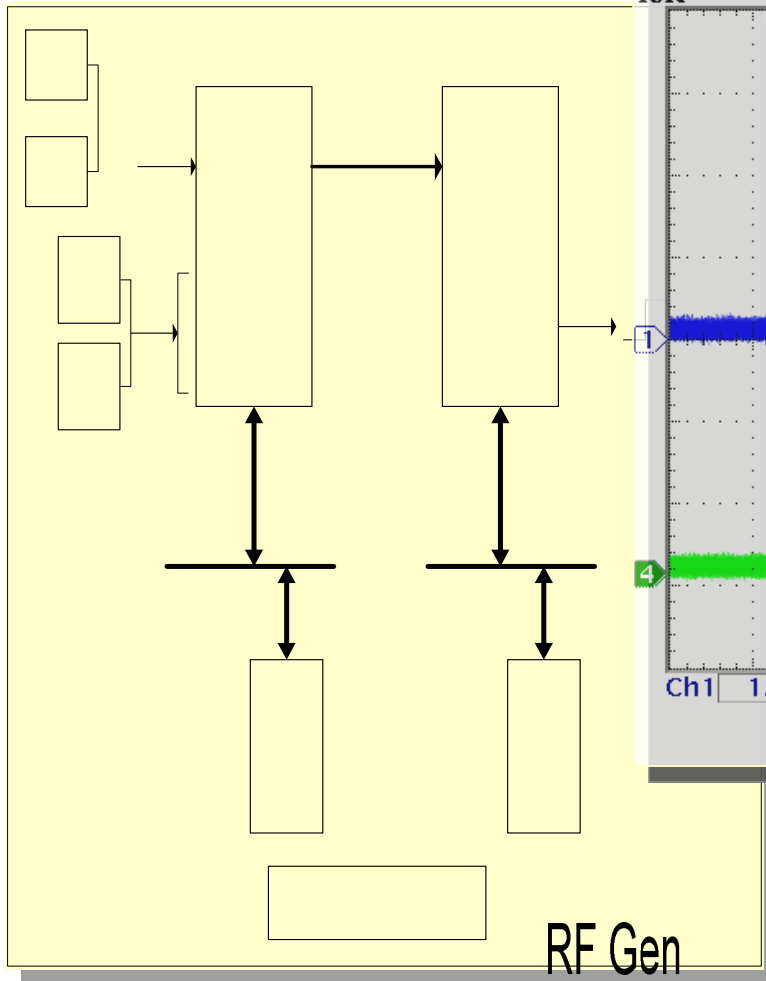
MP01 PNET Bits

Total	102912323	Time Slot Sync Error Counts:	
Rollover of Total	0	Time Slot	0
Invalid Waveform	0	Time Slot Pattern	0
Total (ISR) Writes	102912323	Time Slot/Pattern Mismatch	0
Rollover of Writes	0	Mod 720 Sync Error	0
ISR Overwrites	0	Pulse ID Sync Error	0
ISR Lock Errors	0	Pulse ID Rollover	786
Rate (Hz)	360.0	Sequence RAM Busy	0
Seq Ram Lock Errors	0	Seq RAM Mode Errors	0
Seq Ram Invalid Data	24576	Sequence RAM Active	0
SW Fiducial (Test only)	Off		

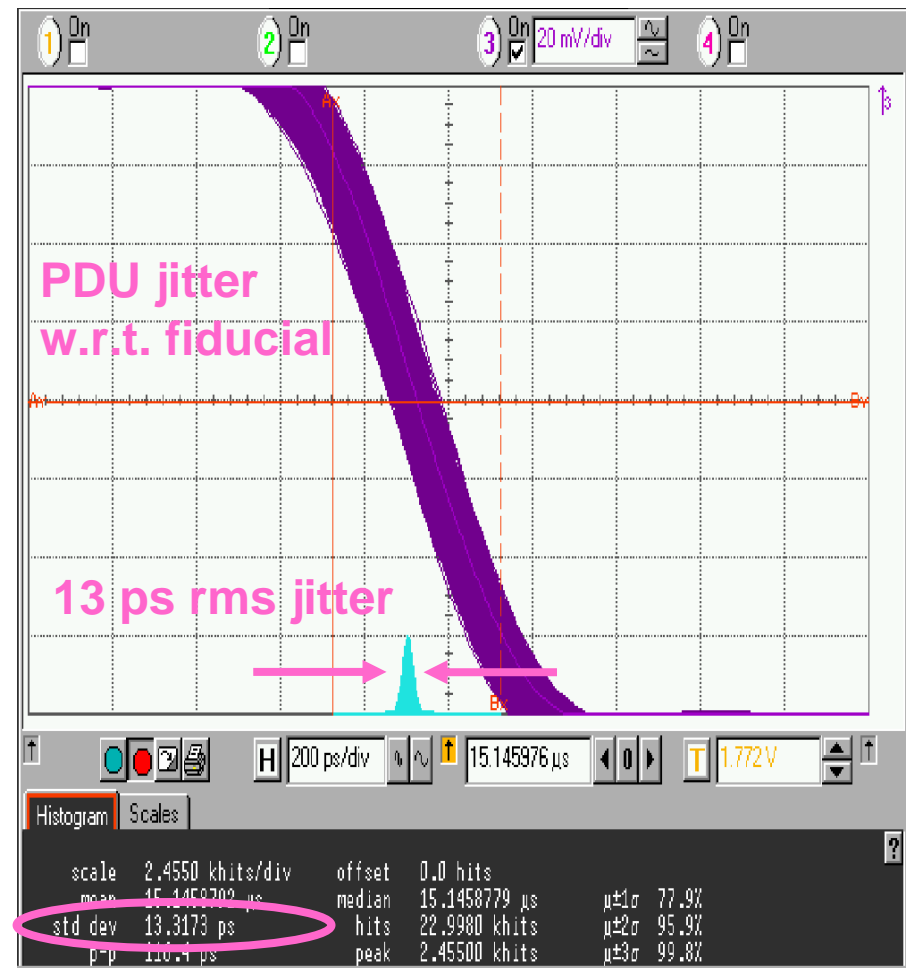
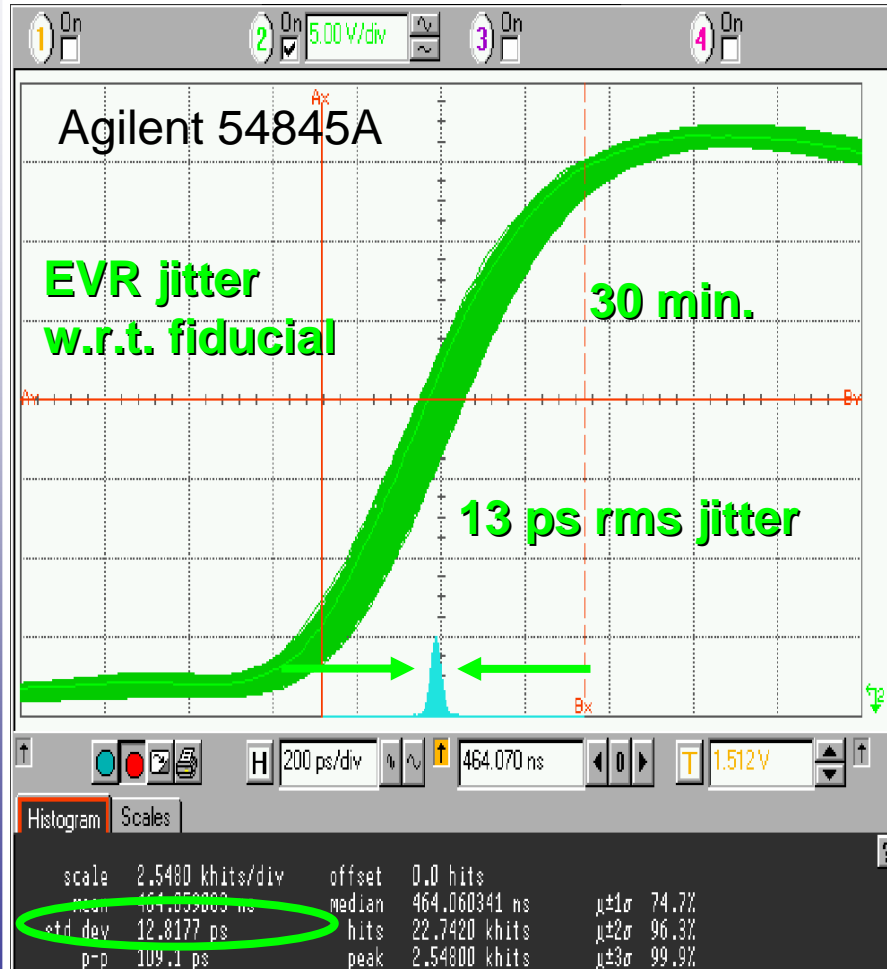
Processing Time (us)

	Average	Std Dev	Maximum*	* Since Reset
	97.6	13.8	356.2	
Start Time Diff		Minimum*	Maximum*	
		2655.0	2899.9	

Hardware Test Stand



Timing Jitter Test Results



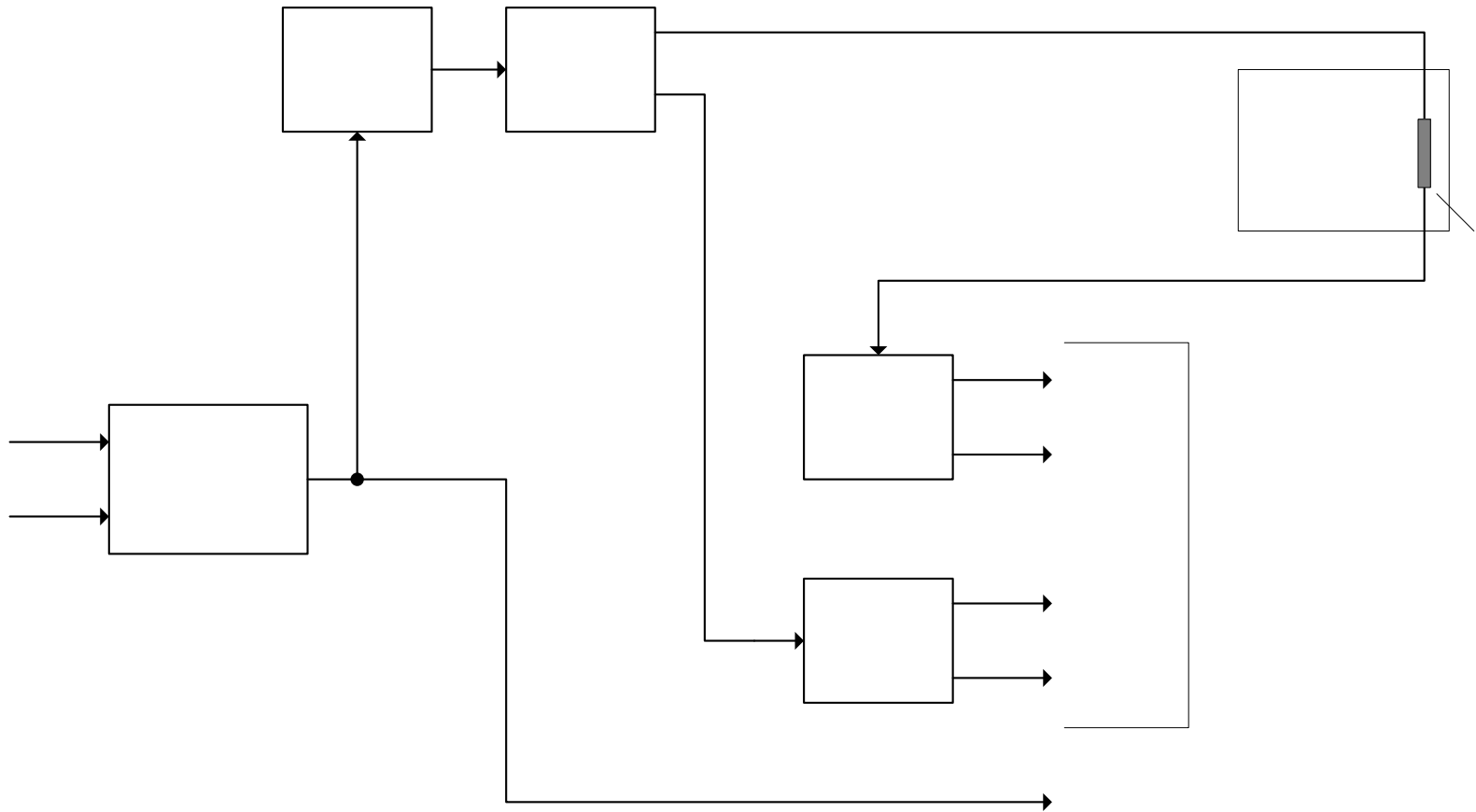
Event System HW: Long-Haul Dist.

- For the next phase, the biggest challenge is Long-Haul distribution of timing data via the Fiber-Optical (F-O) Links
- Why?
 - MRF Event System is designed around Multi-Mode SFP (Small Form-Factor Pluggable) F-O links which allow a maximum fiber length of ~300 meters
 - Our requirements include runs of several Kilometers (at least)
 - Cannot daisy-chain the event F-O links: exceeds the jitter budget
 - Temperature effects on long fibers – drift, but how bad?

Event System HW: Long-Haul Dist.

- Proposed Solution: New HW and some testing
- Single-Mode, pin-compatible SFP modules are commercially available (Agilent ACFT-57R5)
 - All us to go ~10KM
 - Should plug right into our event system HW
- Still does not solve temperature-induced phase-drift problem
 - Propose to solve by either/and:
 - Running Long Fiber in temperature-controlled environment
 - Re-Syncing EVRs to a locally-distributed 119MHz source
- Long-haul fiber test:
 - Function of Single-Mode SFP Modules
 - Drift, Trigger time jitter, Phase Noise

Event System – Long-Haul Fiber System Test



Issues and Tasks

- Outstanding problem (presumably software) where CPU hangs when EVR interrupts are enabled. Some IOCs running without interrupts (hardware triggers but without timestamps, BSA, or event code IRQs).
- Outstanding bug with IRQ processing on VME EVRs
- Software not yet in place to handle hardware and communication errors.
- Changing an event code for a specific trigger requires a change in the delay to trigger at the same time – need database to automate the change
- Need generic timing delay scan software that works for most device types
- Need to get status of RF clock into the system (external interface)
- Ability to change trigger attributes on a pulse-by-pulse basis using simple conditional expressions

Wish List

- When 2 event codes trigger a device on the same pulse, the second event restarts the delay. Wish the second event would be ignored instead.
- Interrupt from the EVG on fiducial trigger (AC line trigger)