Timing and Event System

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Outline

- Overview – HW and Reqts
- Hardware Test Stand
- Long-Haul Fiber Issues and Plans
- Outstanding Software Issues and Tasks
- Wish List

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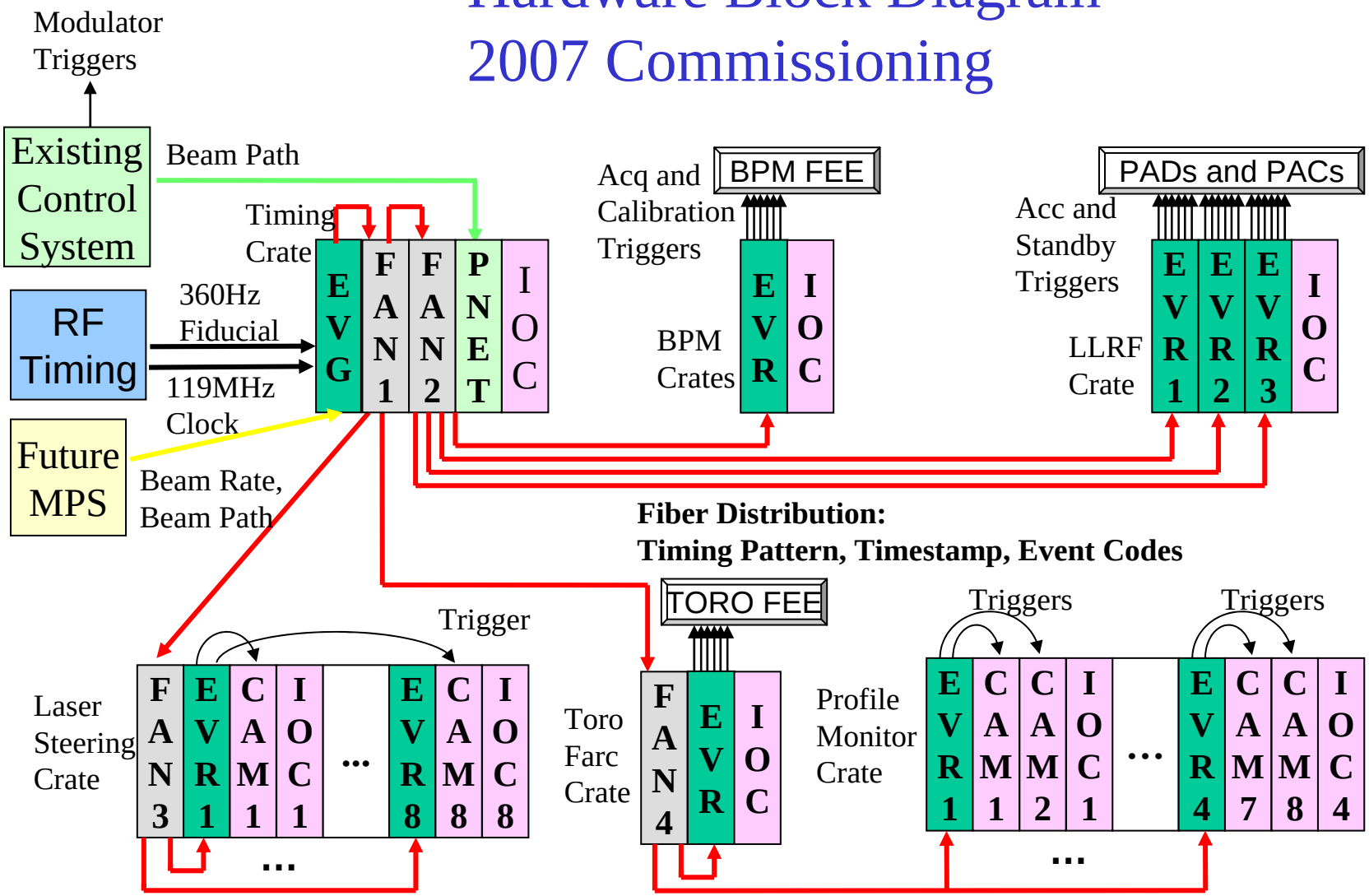
Hardware Block Diagram
2007 Commissioning



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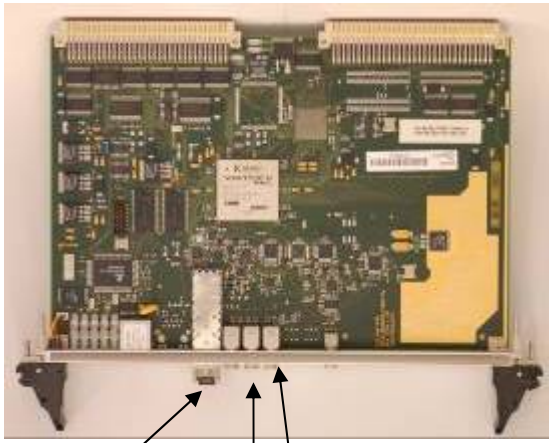
Micro-Research Finland Oy

Event Generator (EVG-200)



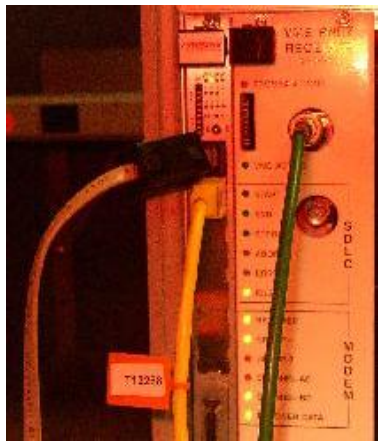
SFP transceiver
• Optical signal to EVRs (fan-outs)

RF input
• Event clock
• divided from RF
• /1*,/4, ... /12

Line syncronisation input
360 Hz

*SLAC addition

SLAC PNET Receiver



- Receives the MPG broadcast sent to SLC micros and passes it to the EVG

EVR Fan Out module

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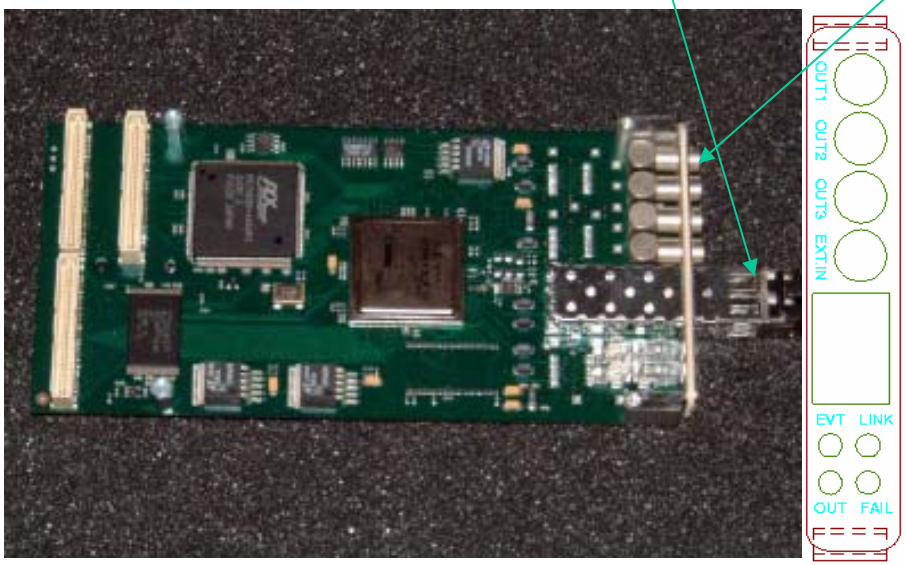
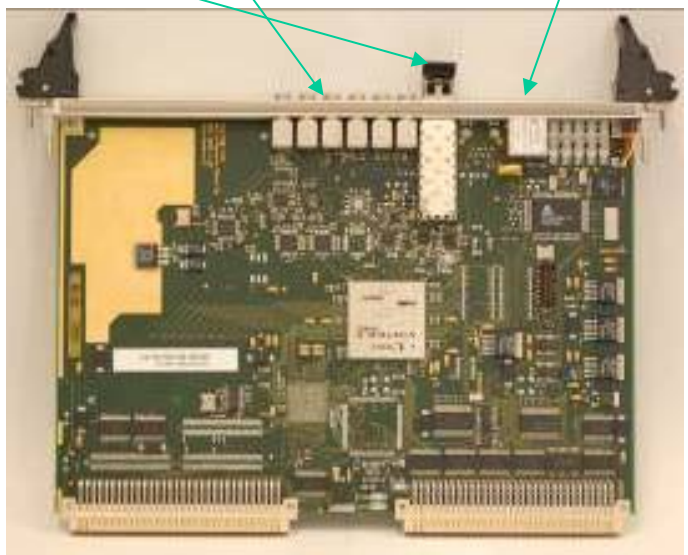
SFP transceiver
• Optical signal from EVG (or fan-out)

Programmable outputs
• 5(3) TTL level
• 2 LVPECL level
External trigger input

Recovered RF output



Event Receiver – PMC version



Event Receiver (EVR-200-RF)

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Modifications to EVG

- 119MHz clock input
  - In the absence of a ÷1 input, a daughterboard was made containing a clock receiver IC to allow us to input 119MHz directly
- EVG AC-line input
  - 360Hz fiducial input was rerouted with firmware change to avoid addition of jitter from internal 10 kHz clock and phase shifter

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Tallies for 2007, Plans for Next Phase

- # EVRs = 31 installed (mostly PMC)
  - Add 60 more EVRs - 34 VME, 26 PMC
- # IOCs with EVRs = 28
  - Add 40 more IOCs with EVRs
- # EVR Fanouts = 4
  - Add 5 more fanouts (1 every 200m)
- # Hardware Triggers = 120+
  - All TTL except 2 NIM triggers for QDCs
  - Most require short cables (except LLRF)
  - Add ? more

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Timing Requirements

Maximum trigger rate	360 Hz
Clock frequency	119 MHz
Clock precision	20 ps
Coarse step size	8.4 ns ± 20 ps
Delay range	>1 sec
Fine step size	20 ps
Max timing jitter w.r.t. clock	2 ps rms
Differential error, location to location	8 ns
Long term stability	20 ps

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Event System Requirements

- Event Generator IOC:
  - Send out proper event codes at 360Hz based on:
    - PNET pattern input (beam code and bits that define beam path and other conditions)
    - Add LCLS conditions such as BPM calibration on off-beam pulses , diagnostic pulse etc.
  - Future – event codes also based on new MPS and user input
  - Send out system timestamp with encoded pulse ID from PNET
  - Send out PNET pattern to be used by SLC-aware IOCs
  - Manage user-defined beam-synchronous acquisition measurement definitions (event definition or EDEF)
  - Check for match between user EDEFs and input PNET pattern at 360Hz and tag matches in outgoing pattern

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Event System Requirements, cont

- Event Receiver IOC:
  - Set trigger delays, pulse widths, and enable/disable via user requests (not yet done on a pulse-by-pulse basis)
  - Set event code per trigger (triggering done in HW when event code received)
  - Receive event pattern 8.3 msec before corresponding pulse
  - Perform beam-synchronous acquisition based on tags set by EVG in the event pattern
  - Perform beam-synchronous acquisition for the SLC-aware IOC based on the PNET part of the event pattern
  - Process pre-defined records when specific event codes are received (not yet available – bug!)

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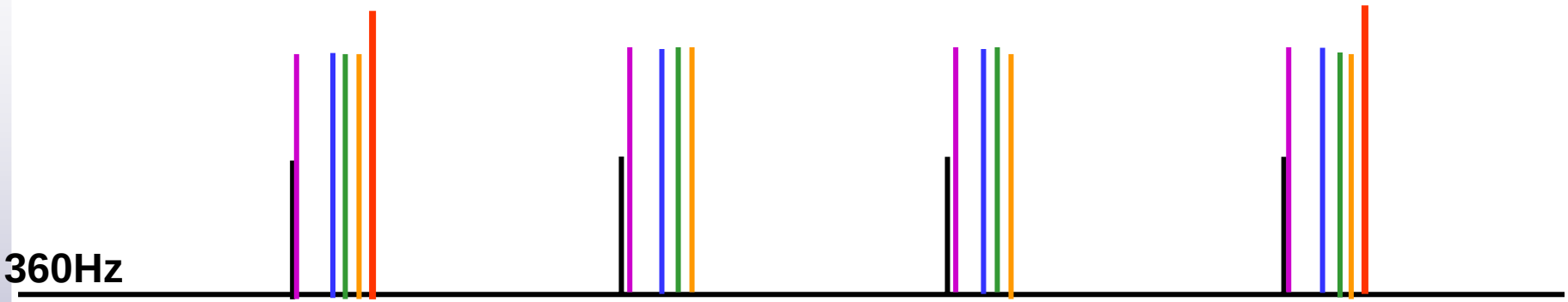
EVG Event Time Line – 4 Fiducials



Time (msec) 0 1.0 2.8 5.6 8.3 9.3

HW starts sending event codes, starting with fiducial event code: R0 R1 R2 R3

Receive Fn+3 PNET, determine Fn+3 LCLS pattern, and advance pipeline (n-2->n-1->n): P0 P1 P2 P3

Send LCLS pattern: L0 L1 L2 L3

Set Event Codes in Other RAM based on the last patterns for Fn+1: E1 E2 E3 E4

120Hz BEAM: B-3 B0

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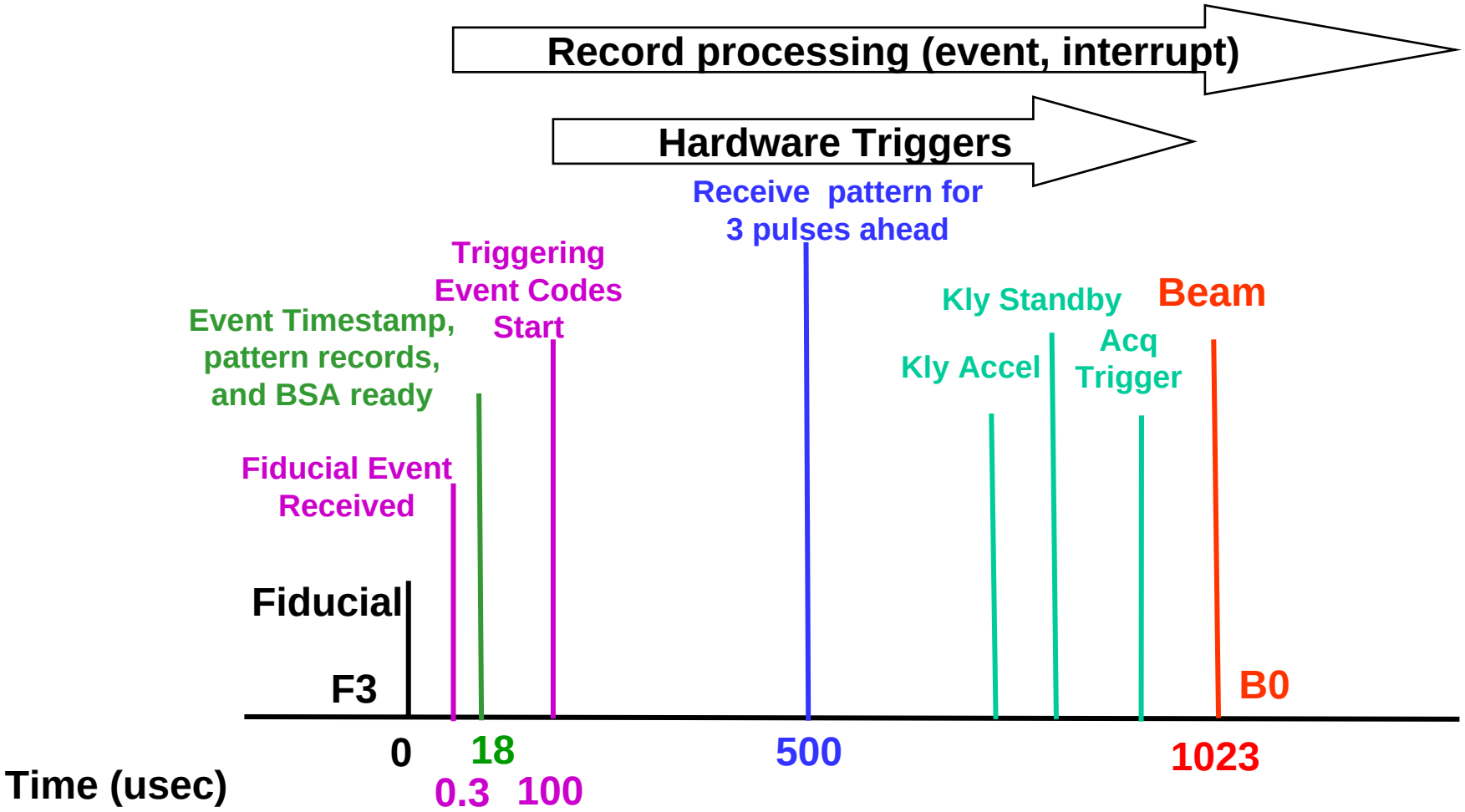
Trigger Event Time Line – 1 Beam Pulse (B0)



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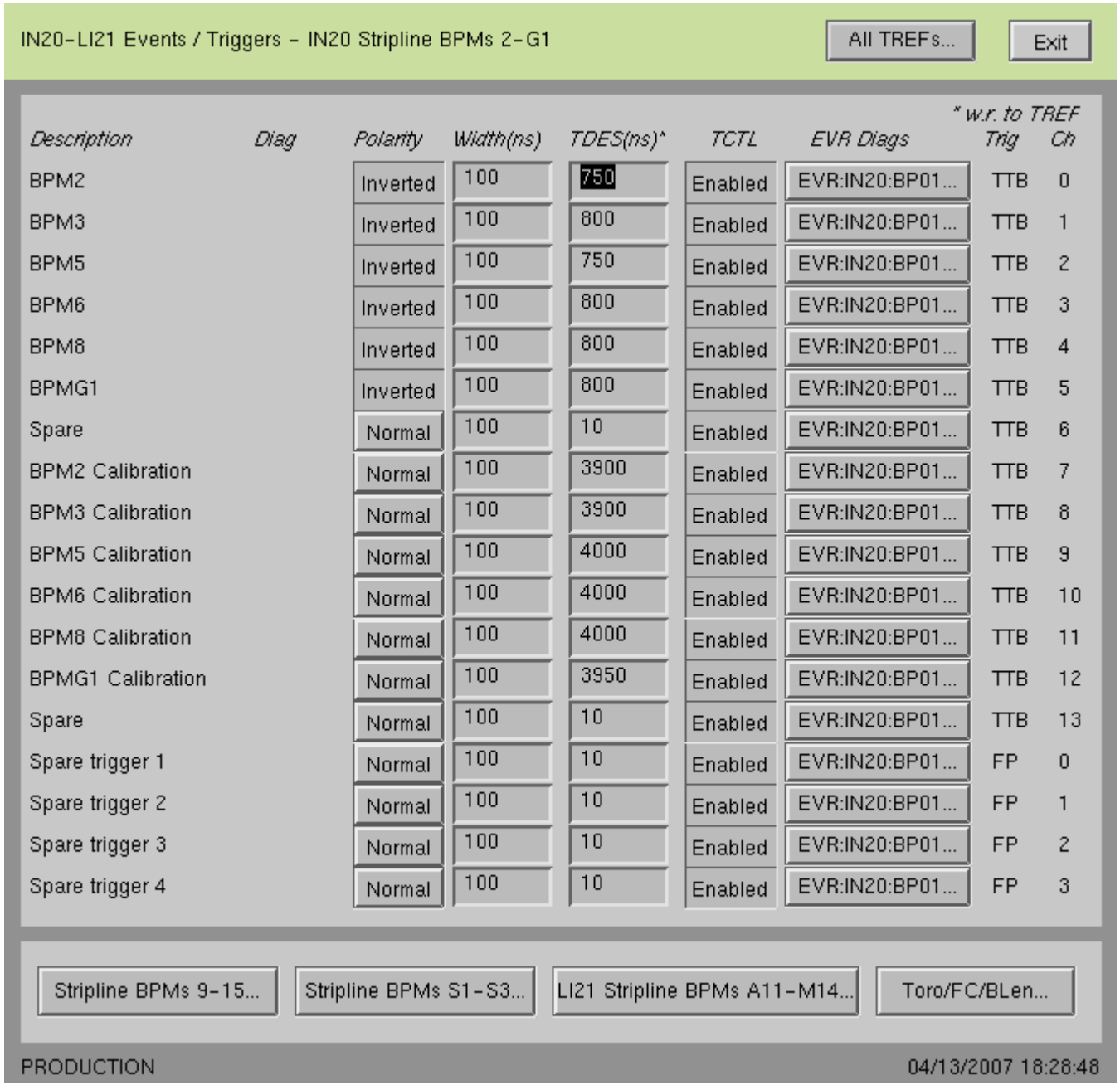
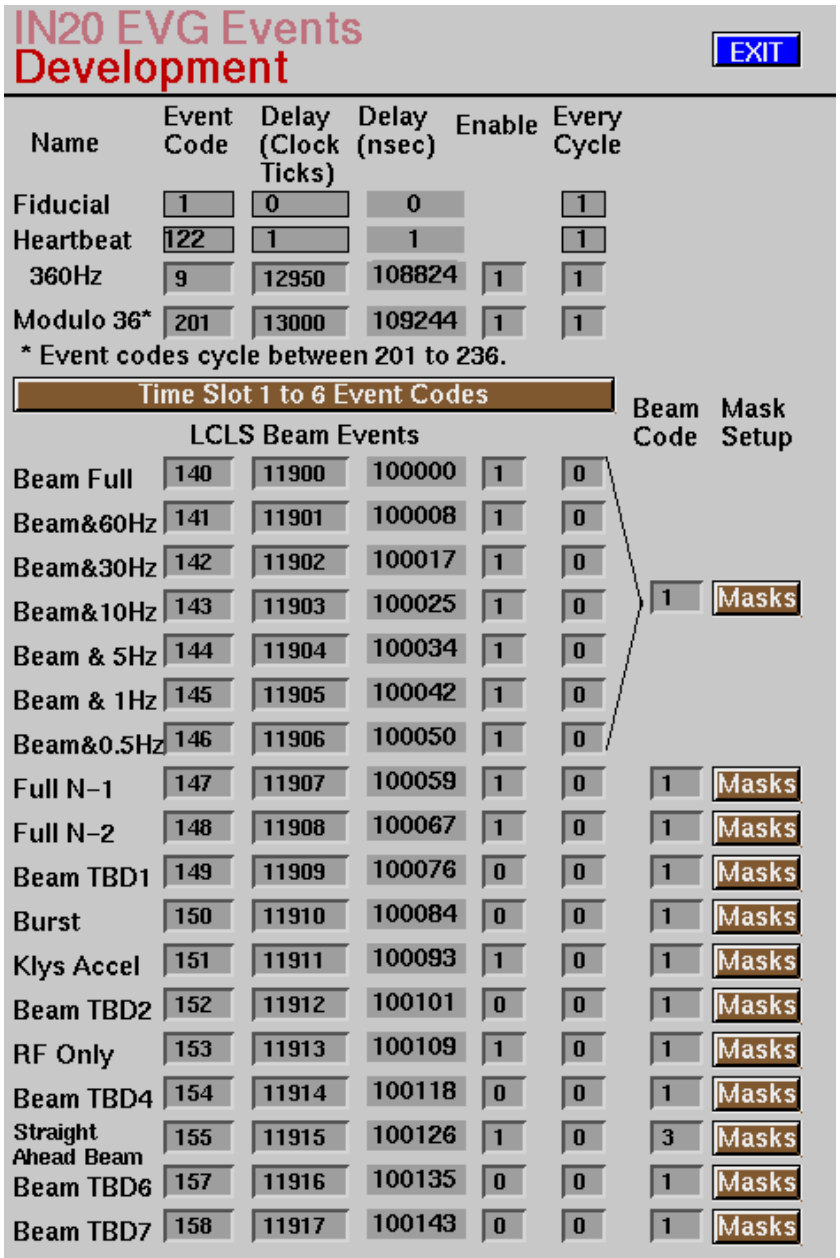
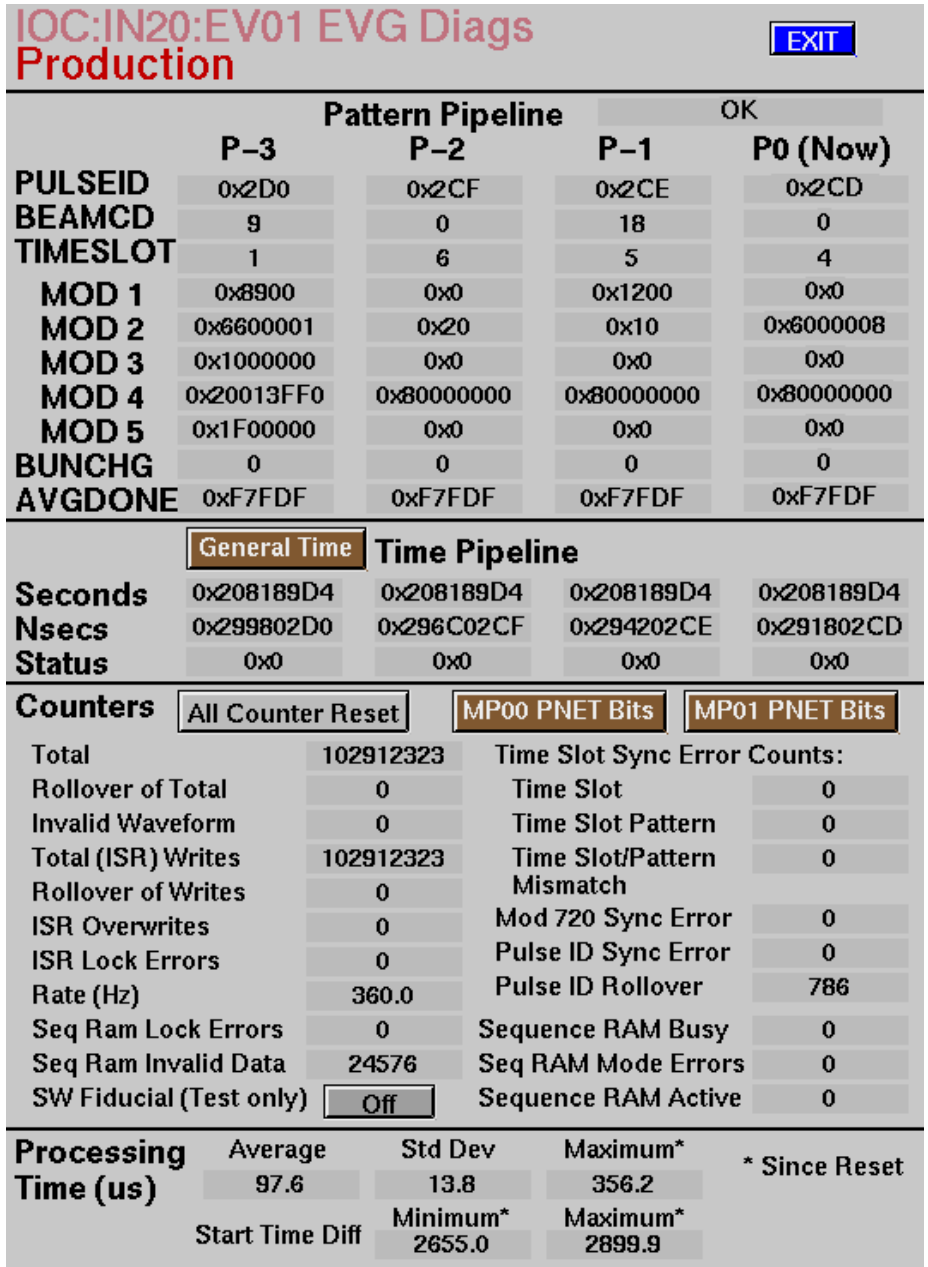
Trigger Control Display

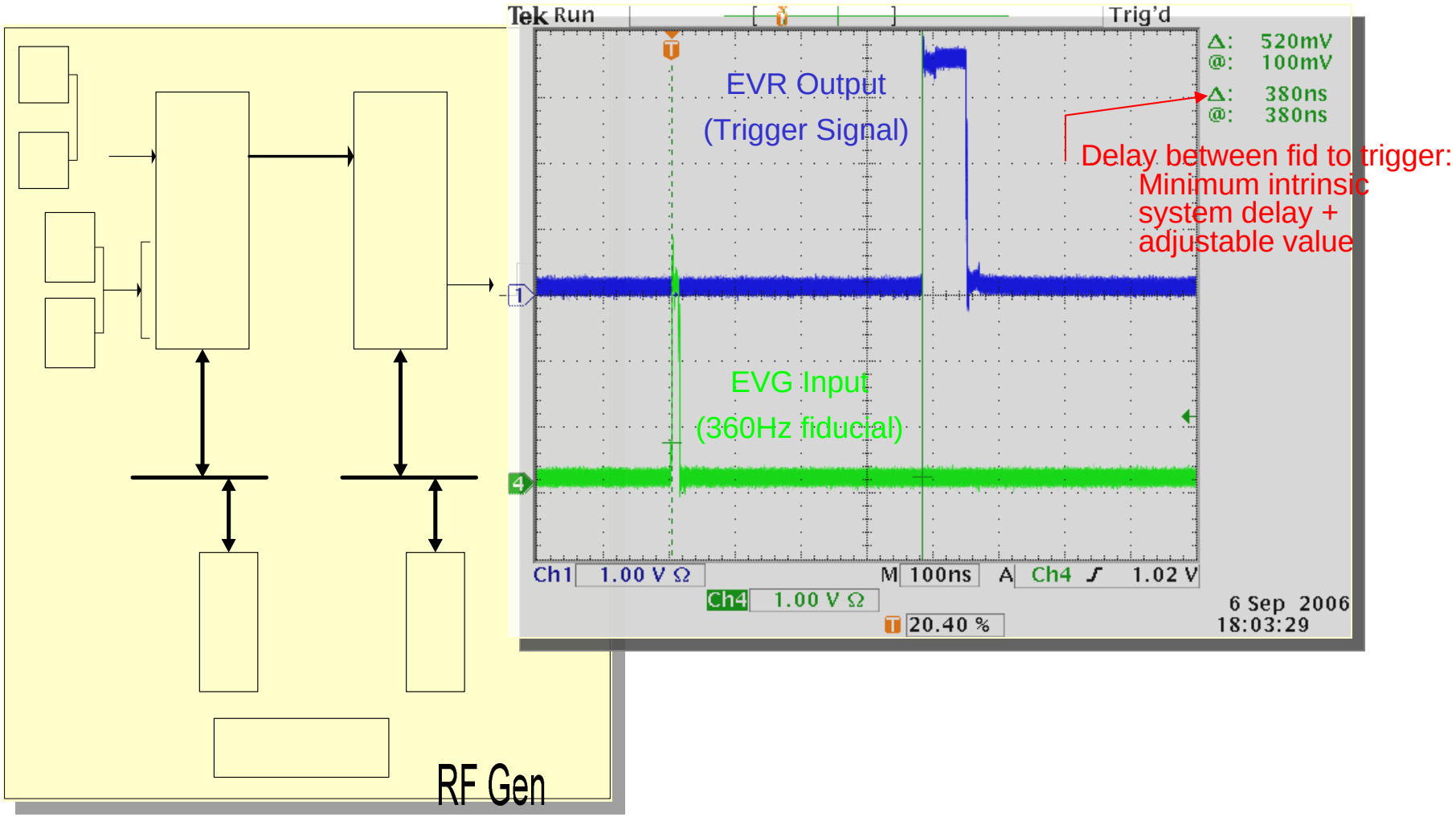


EVG Displays





Hardware Test Stand



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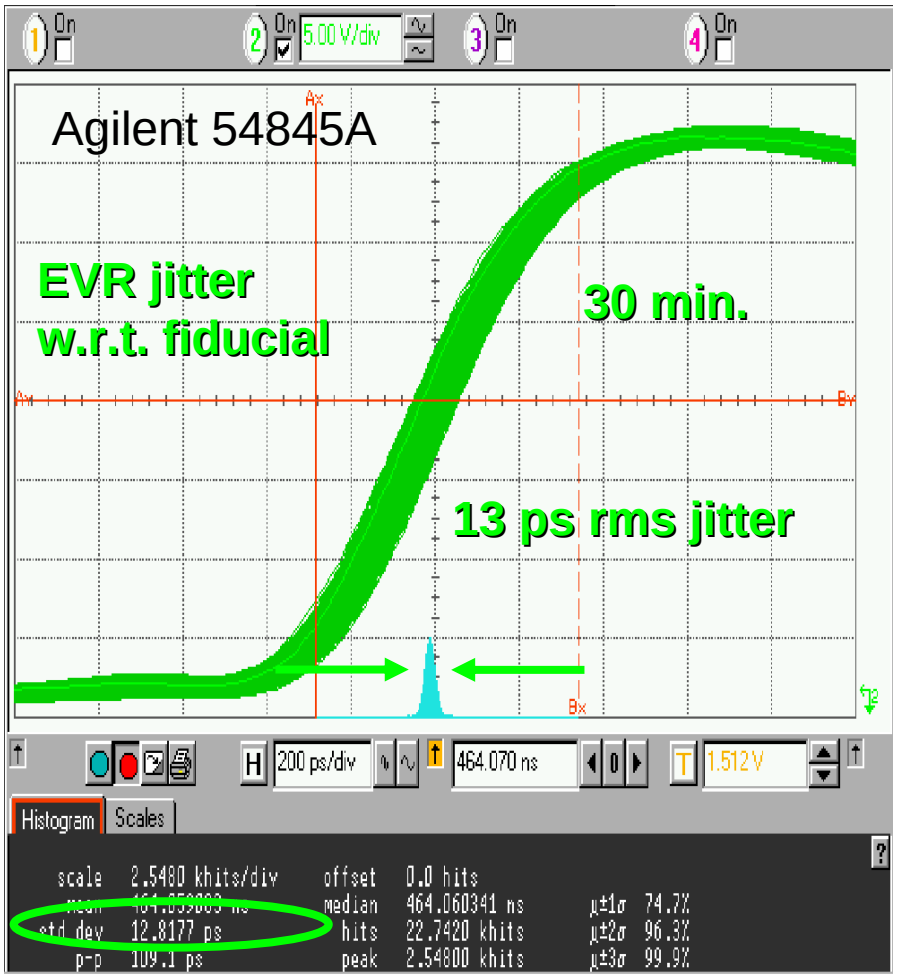
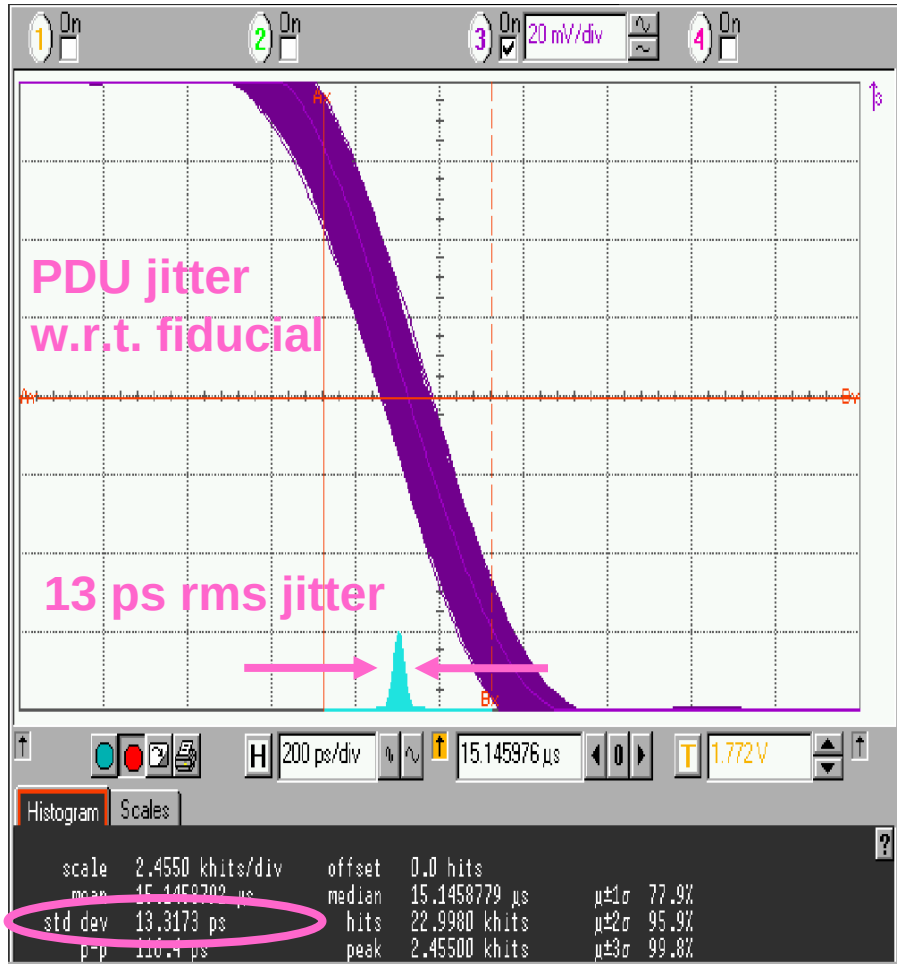
Timing Jitter Test Results





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Event System HW: Long-Haul Dist.

- For the next phase, the biggest challenge is Long-Haul distribution of timing data via the Fiber-Optical (F-O) Links
- Why?
  - MRF Event System is designed around Multi-Mode SFP (Small Form-Factor Pluggable) F-O links which allow a maximum fiber length of ~300 meters
  - Our requirements include runs of several Kilometers (at least)
  - Cannot daisy-chain the event F-O links: exceeds the jitter budget
  - Temperature effects on long fibers – drift, but how bad?

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Event System HW: Long-Haul Dist.

- Proposed Solution: New HW and some testing
- Single-Mode, pin-compatible SFP modules are commercially available (Agilent ACFT-57R5)
  - All us to go ~10KM
  - Should plug right into our event system HW
- Still does not solve temperature-induced phase-drift problem
  - Propose to solve by either/and:
    - Running Long Fiber in temperature-controlled environment
    - Re-Syncing EVRs to a locally-distributed 119MHz source
- Long-haul fiber test:
  - Function of Single-Mode SFP Modules
  - Drift, Trigger time jitter, Phase Noise

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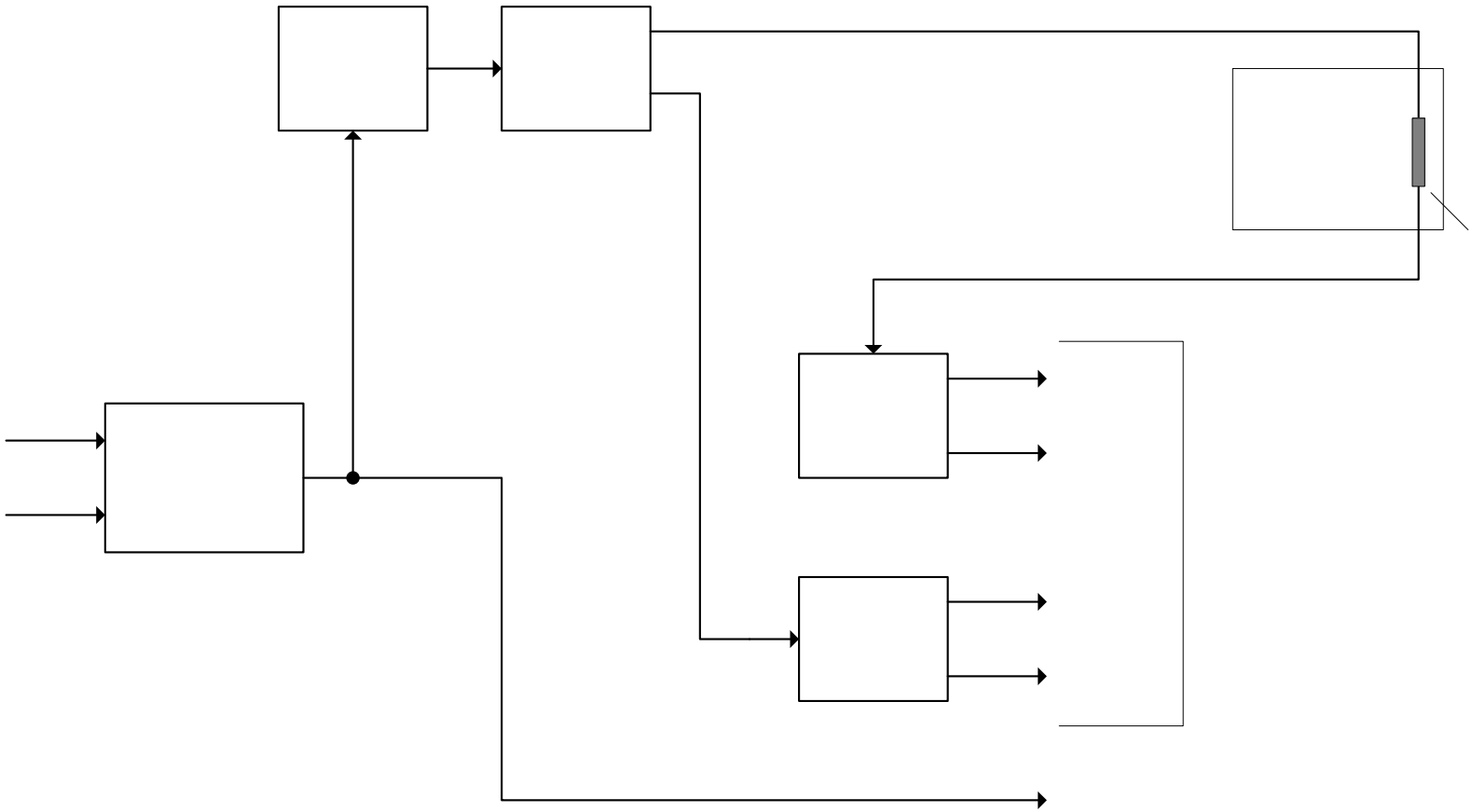
Event System – Long-Haul Fiber System Test



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Issues and Tasks

- Outstanding problem (presumably software) where CPU hangs when EVR interrupts are enabled. Some IOCs running without interrupts (hardware triggers but without timestamps, BSA, or event code IRQs).
- Outstanding bug with IRQ processing on VME EVRs
- Software not yet in place to handle hardware and communication errors.
- Changing an event code for a specific trigger requires a change in the delay to trigger at the same time – need database to automate the change
- Need generic timing delay scan software that works for most device types
- Need to get status of RF clock into the system (external interface)
- Ability to change trigger attributes on a pulse-by-pulse basis using simple conditional expressions

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Wish List

- When 2 event codes trigger a device on the same pulse, the second event restarts the delay. Wish the second event would be ignored instead.
- Interrupt from the EVG on fiducial trigger (AC line trigger)

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