

Image Processing for the LCLS XAMPS Detector & Firewire Cameras on RTEMS

RTEMS Primer and Workshop

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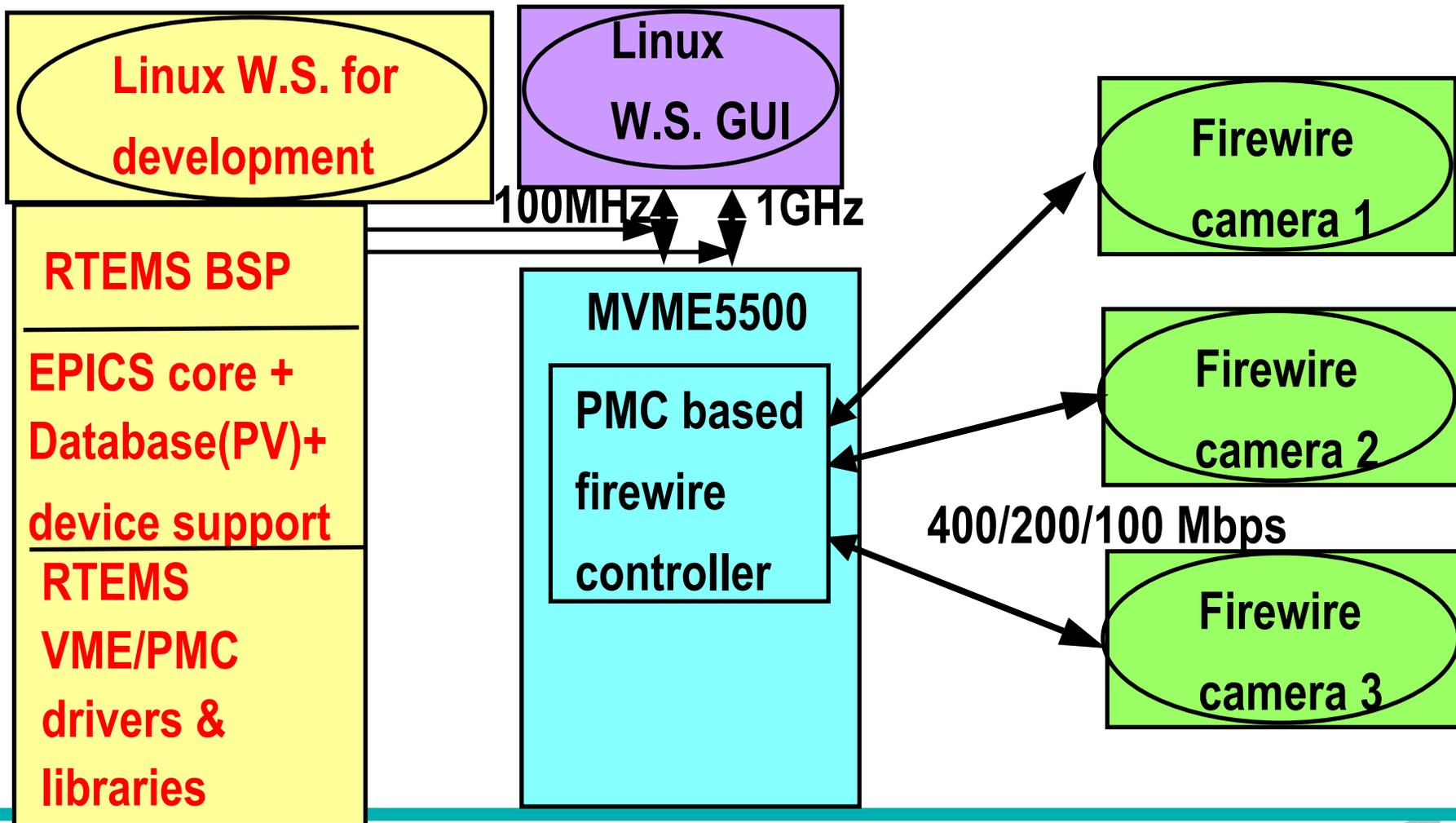
Overview

- ◆ Introduction
- ◆ Status of the image processing for firewire cameras
- ◆ Design of image processing for the LCLS XAMPS detector
 - ◆ Requirements of the LCLS XAMPS detector
 - ◆ The DAS designs of the LCLS XAMPS detector
 - ◆ System advantages
 - ◆ Data Storage
 - ◆ End user options
- ◆ The prospect of data acquisition on EPICS
- ◆ Conclusion
- ◆ Acknowledgement

Introduction

- ◆ **Two image processing projects**
 - ◆ **Project #1: The PMC based firewire controller in a MVME500 EPICS/RTEMS IOC for firewire cameras.**
 - ◆ **Project #2: The Data Acquisition System (DAS) that I designed for the LCLS XAMPS detector.**
- ◆ **The prospect of image processing on EPICS**
 - ◆ **Real-time data display at a rate $\gg 10\text{HZ}$ for a $1024 \times 1024 \times 2$ bytes of image.**
 - ◆ **Fast data storage for a later-on data analysis or video playback.**

Image processing for firewire cameras



Status of the image processing on firewire

- ◆ The RTEMS device driver for the firewire controller and libraries for the IIDC based cameras are written and mostly interfaced to the EPICS device drivers developed by the Diamond Light Source. The result of the EDM display is shown in the next page.
- ◆ The interface software among the layers of RTEMS firewire drivers, RTEMS-IIDC libraries, and EPICS device drivers for image transfer is yet to be completed.

EDM display

The screenshot shows a window titled `/home/feng/Mr1394/Rx-y/Mr1394App/opi/edl/Mr1394.edl`. On the left, there is a list of camera settings. On the right, there is a large black rectangular area, likely a camera feed that is currently off. Below the black area are two empty plots with x-axes labeled 'Xdist' and 'Ydist', both ranging from 0 to 1600.

Number of Cameras:	1
Vendor:	Point Grey Research
Model:	Flea FLEA-HIBW
Format:	1
Set Format:	1
Mode:	6
Set mode:	6
Available Format, Mode:	7,2 7,1 7,0 1,7 1,6 1,5
Formats/modes	32
Frame Width:	800
set frame width:	0
Frame Max Width:	800
Frame Width offset:	0
Frame set width offset:	0
Frame Height:	600
set frame height:	0
Frame Max Height:	600
Frame Height offset:	0
Frame Set Height offset:	0
Frame Size:	480000
Min Frame Rate:	3.75
Max Frame Rate:	240.00
Frame Rate:	3.75
Set Framerate	3.75
Brightness:	0.00
Set Brightness	0
X max	0.00
X average	0.00
X width	0.00
X Position	0.00
Y max	0.00
Y average	0.00
Y width	0.00
Y position	0.00

Image processing for the LCLS XAMPS detector

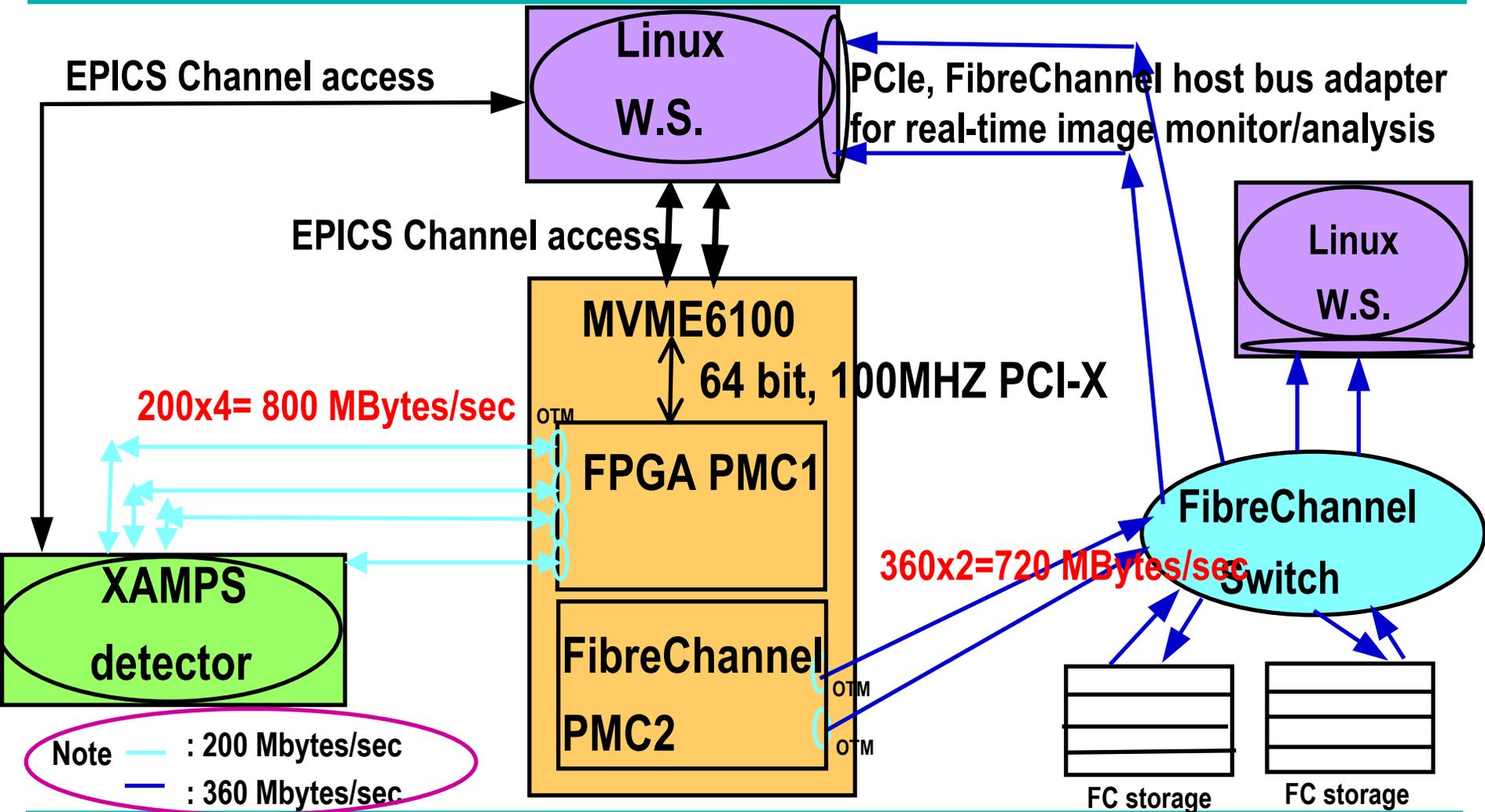
Following pages

Requirements of the LCLS XAMPS detector

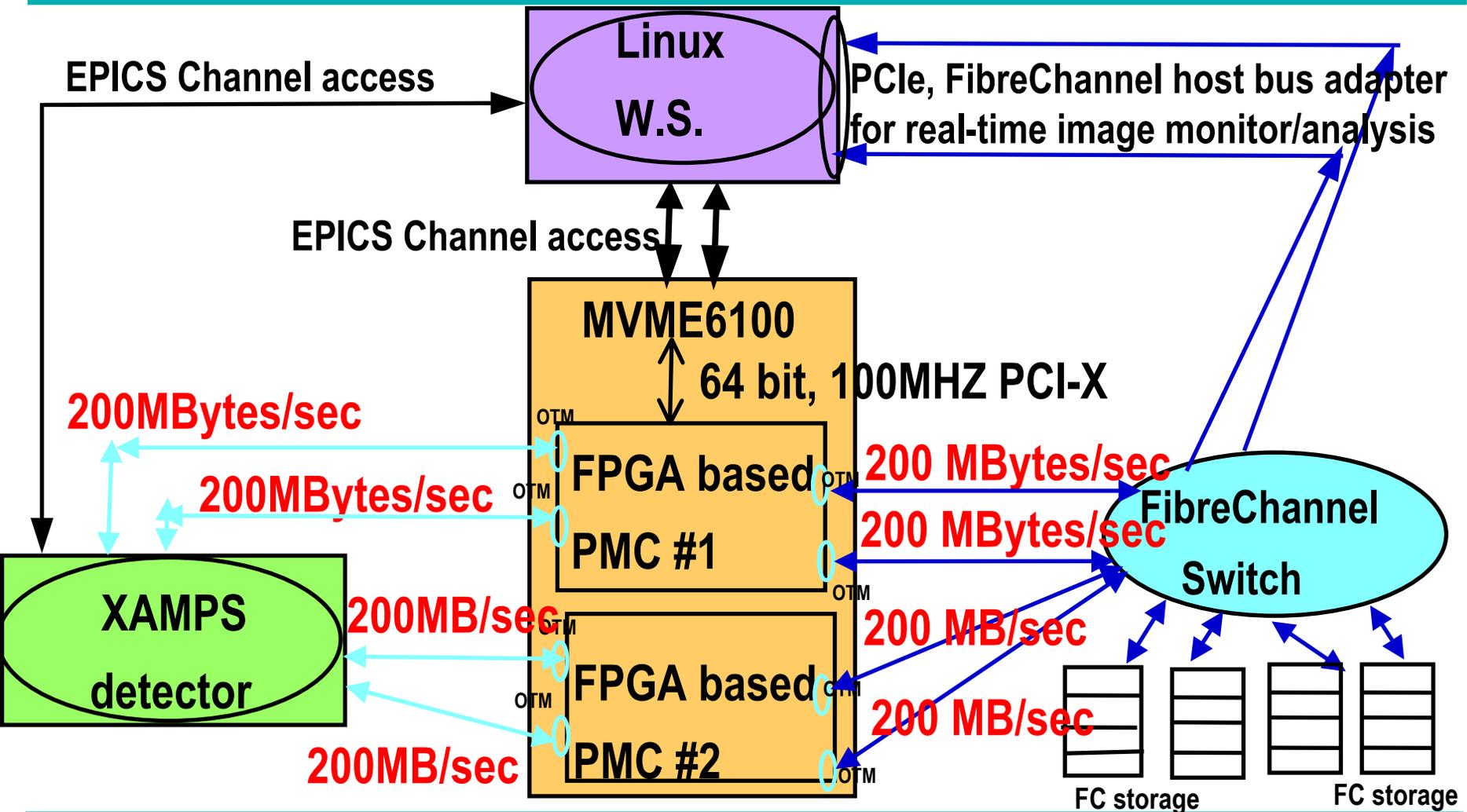
- ◆ **Detector Arrays: 1024 x 1024 pixels.**
- ◆ **Resolution of the ADCs: 14 bits (two bytes).**
- ◆ **Triggering rate: 120 HZ.**
- ◆ **----> Data Rate: 252 MBytes/sec (1024x1024x2x120).**
- ◆ **The scope of work: reading in and storing of the detector's data at a rate faster than 252 MBytes/sec for a 7days/24 hours operation.**
- ◆ **Bonus**
 - ◆ **The system provides an option for a remote fast data analysis/display/playback.**

DAS design 1

one FPGA PMC + one conventional FC PMC



DAS design 2 – two FPGA based PMCs



Which DAS design ?

- ◆ The DAS design 1 is a less risky approach even though it is slightly slower. The only restriction is that it comes with either two ports of 2 Gbps FCs or two ports of 4 Gbps FCs.
- ◆ It depends on what the worst case of the disk-write rate of 2Gbps and 4Gbps FC RAIDS is and the actual performance of the FC PMC card. Sometimes the hard truth could be discovered only through one's own test.

System Advantages -1

- ◆ **FPGAs have demonstrated the capability to deliver at least one order of magnitude performance gain over general-purpose processors (e.g. PowerPC) by offering many data paths and the ability to customize the memory architecture to the problem. The Commercial-Off-The-Shell (COTS) generic FPGA PMC1 contains two independent banks of DDR SDRAM facilitating parallel operations between the data acquisition and data storage.**
- ◆ **The protocol between the detector and the FPGA of the system provides a fast, and low-latency link at a data rate up to 200 Mbytes/sec per lane. Four lanes of the bandwidth will deliver 800 Mbytes/sec of throughput.**

System Advantages – 2

- ◆ The optical link between the detector and the VME crate can be extended up to 10 km in distance. The Fibre Channel cable to be used for the data storage can operate over a distance of 1000 feet. The cables for both kinds of links are lightweight.
- ◆ The dual-ported Fibre Channel (FC) PMC is capable of transferring the data to the FC storage at a rate of 760 Mbytes/sec, when both ports are used simultaneously, or 400 Mbytes/sec per port when one port is active at a time. [More advantages of FC storage is described at: Data storage.](#)

System Advantages – 3

- ◆ It consists of a MVME6100 Board equipped with a CPU @ 2926.8 Million Instructions Per Second (MIPS) and another FPGA embedded processor @ 600 MIPS. The 64 bit, 100 MHz PCI bus will meet the needed bandwidth for fast data transfer to the FC disk. The EPICS/VME Input/Output Controller (IOC) will store each frame of image and EPICS timestamp to the file system of the FC disk RAID at a rate of 120 Hz.
- ◆ The choice of the MVME6100 CPU board, EPICS, and RTEMS is inexpensive, high performance, and conforms to the LCLS Control Group standards.

Data Storage

- ◆ The Storage Area Network (SAN) is a technology utilizing the FC interface and SAN management software to access, or share data stored on multiple storage arrays. The **Fibre Channel Switch** is the “**traffic cop**” of the SAN, not only **managing the access paths** between any host workstation or server, and any storage array on the SAN, but **making the full bandwidth of each storage array available** to each host workstation or server.
- ◆ Each FC storage is dual ported with an independent RAID controller and both ports can be simultaneously used allowing one to read from one port for data analysis and monitor while real-time data is stored via the other.

End user options

- ◆ **Remote fast real-time image analysis/display/playback is available by setting up the SAN:**
 - 1: PCI Express Fibre Channel Host adapter for a PCI Express based PC, which has a device driver developed for Linux.
 - 2: Fibre Channel storage with hot swappable drives.
 - 3: Fibre Channel Switch.
 - 4: SAN management software.
- ◆ **The FC disk RAID's function as a local disk to the Linux workstations which are attached to the SAN facilitating client software reading data off the FC storage for fast image analysis/display/playback. Existing Linux supported video/analysis applications could be used as a display frame work.**

End user options

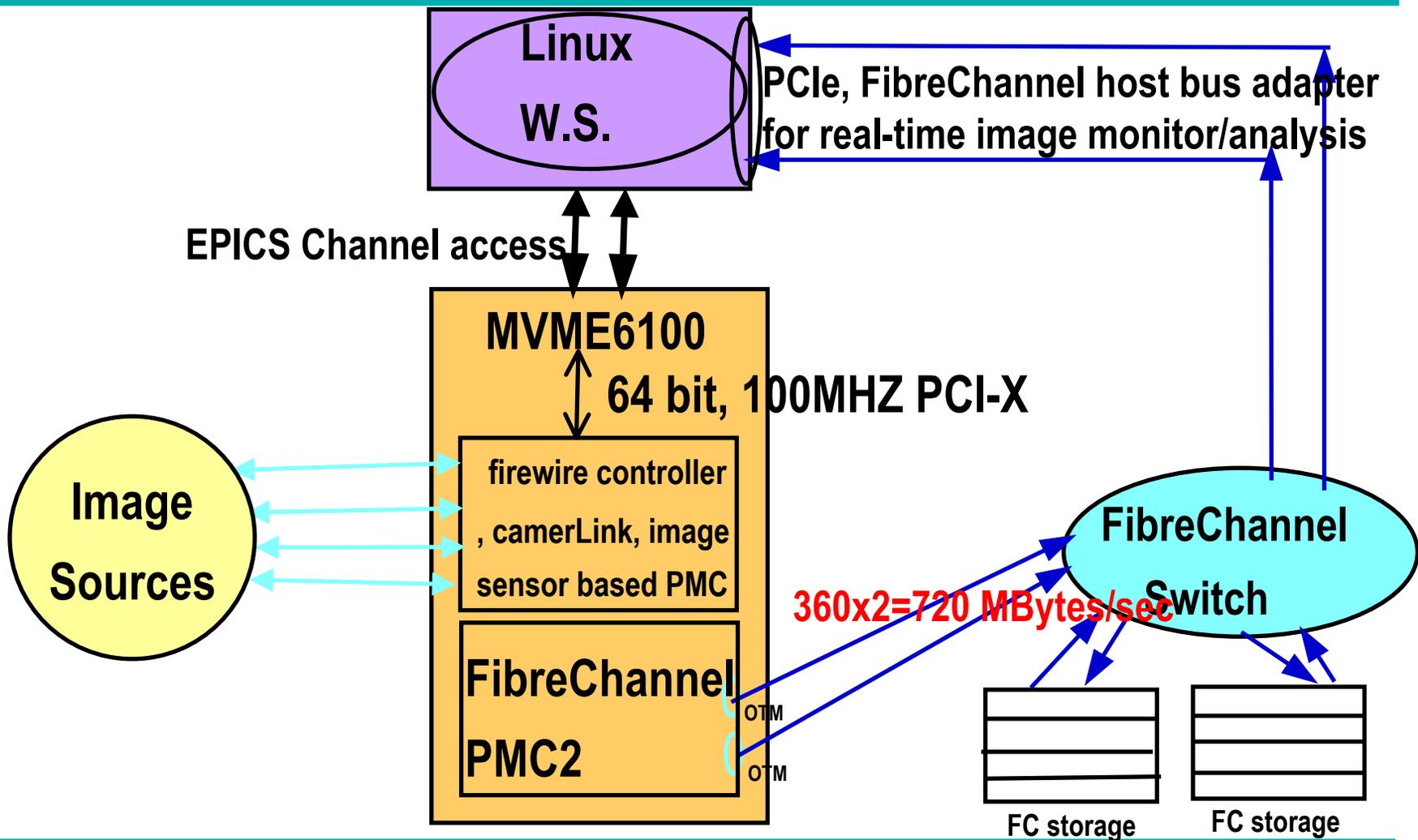
- ◆ The data acquisition system should sustain simultaneous read and write operations at a rate of 300 Mbytes/sec or greater to ensure the data storage and to provide a fast image display on any workstation attached to the SAN at a rate $\gg 10$ HZ for a 1024x1024x2 or larger bytes of image.
- ◆ A slower rate of real-time image display (e.g. the EDM display in page 6) via EPICS channel accesses could be achieved to provide the display especially for a remote host which is not attached to the SAN. Alternatively, one might achieve a faster image display via 10Gbps network links to any client application on a workstation which is attached to the SAN.

The prospect of data acquisition on EPICS

- ◆ The FPGA based PMC1 in page 9 of DAS design 1, could be replaced by any data acquisition PMC, or image sensor based PMC such as a firewire controller, or a camera link, depending on the applications. See the block diagram in next page.
- ◆ The Fibre Channel PMC2 in an EPICS IOC facilitates fast data storage (e.g. 120 to 240 frames/sec) and, when coupled with a PCIe Fibre Channel host adapter on a workstation, the system will provide high bandwidths to the Linux client for a real-time data display at a rate $\gg 10$ HZ for a 1024x1024x2 or larger bytes of image.

A versatile design

one image sensor + one conventional FC PMC



Conclusion

- ◆ The data acquisition system for the LCLS XAMPS detector will meet the requirement and offer optimal end user options. It is the least expensive option explored on the market. It adheres to the LCLS Control Group Standards reducing the future maintenance effort.
- ◆ It adapts the open VME platform, open source EPICS, and FPGA/PMCs, which provides a versatile (e.g. the prospect of DAQ on EPICS), reusable, and modular design facilitating future expansion to deliver higher data acquisition rates, when needed.

Acknowledgement

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