

P0 Feedback Project: Merging EPICS with FPGA's

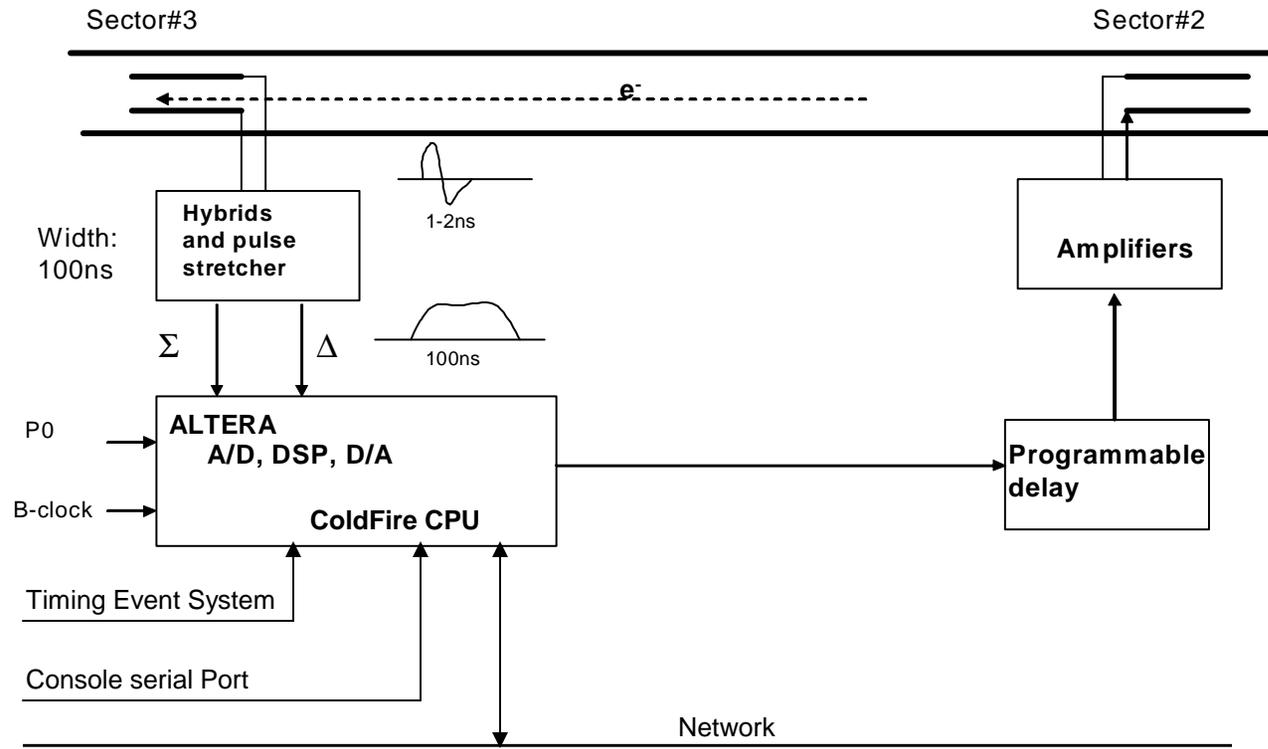
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P0 Feedback Project



- Transverse beam stabilizer
- Turn-by-turn horizontal kick of the 'P0' bunch
- Monitors X-plane, Sum, (Y-plane near future)

P0 Feedback Project

- Project given to me with the following criteria:
 - Use Coldfire CPU
 - Use RTEMS
 - Use Altera's DSP Development Kit
 - Use Altera's SOPC
- Never used any of the above
- Never worked on a DSP project
- And, by the way, they want to install it in 6 months.

- Oddly enough, an opportunity like this wasn't coming from the RF Group.
 - Why change analog to DSP when up-time is around 99%?

P0 Feedback Project

- However, this project was accomplished in two months in light of my other priorities.
- Why
 - because of SOPC
 - because of ASYN
 - because of the DSP kit
 - because of the Coldfire CPU
 - because of EPICS R3.14.8
 - and support from Eric Norum

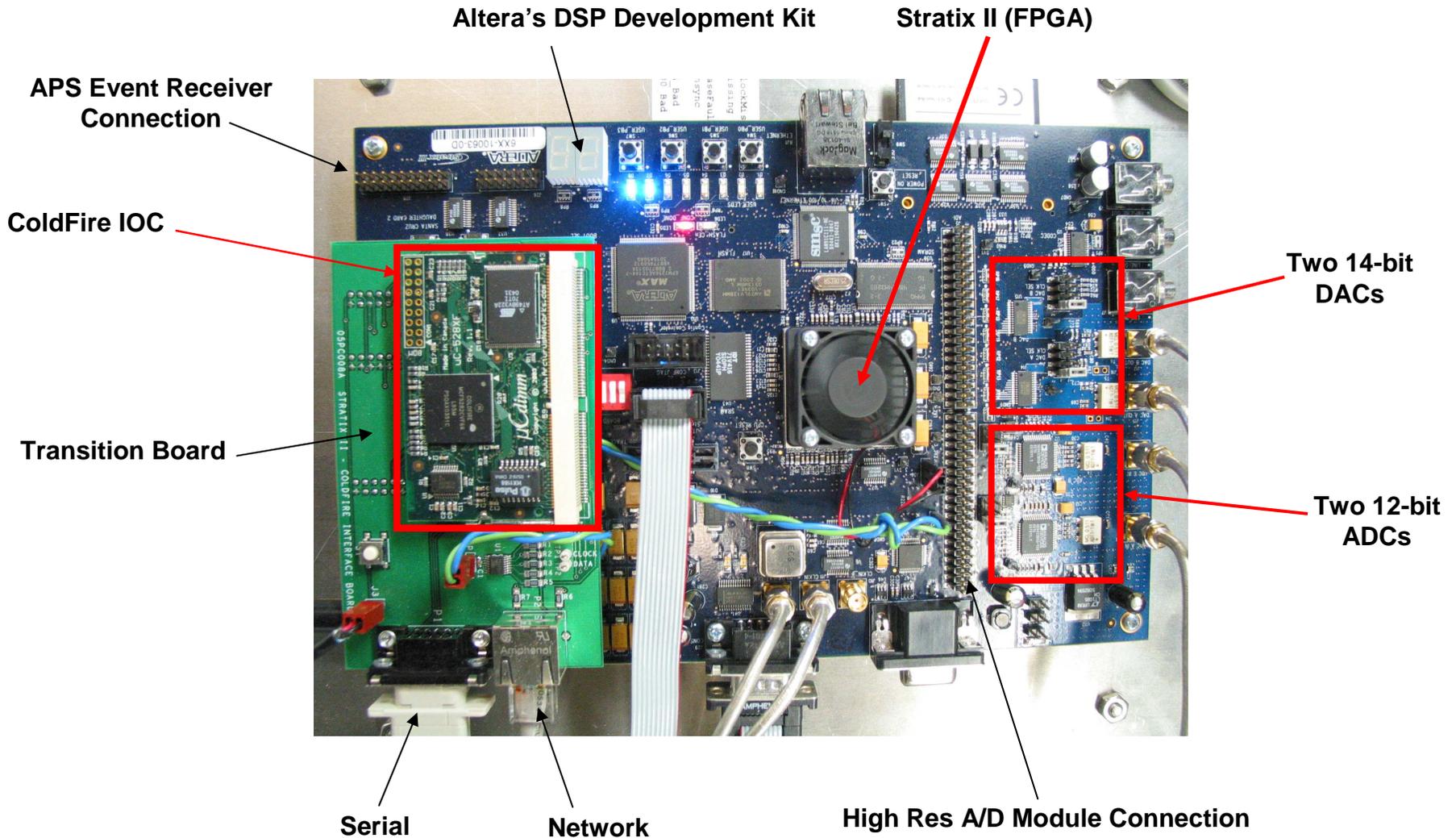
P0 Feedback

- Algorithm: (For single P0 bunch)
 - Read horizontal beam position ADC.
 - Remove ‘DC’ component, selectable HPF.
 - Apply programmable 32-tap FIR filter.
 - Apply programmable delay (up to 1 turn).
 - Write value to DAC.
- Filter coefficients, control bits, raw ADC waveforms are needed as EPICS process variables.

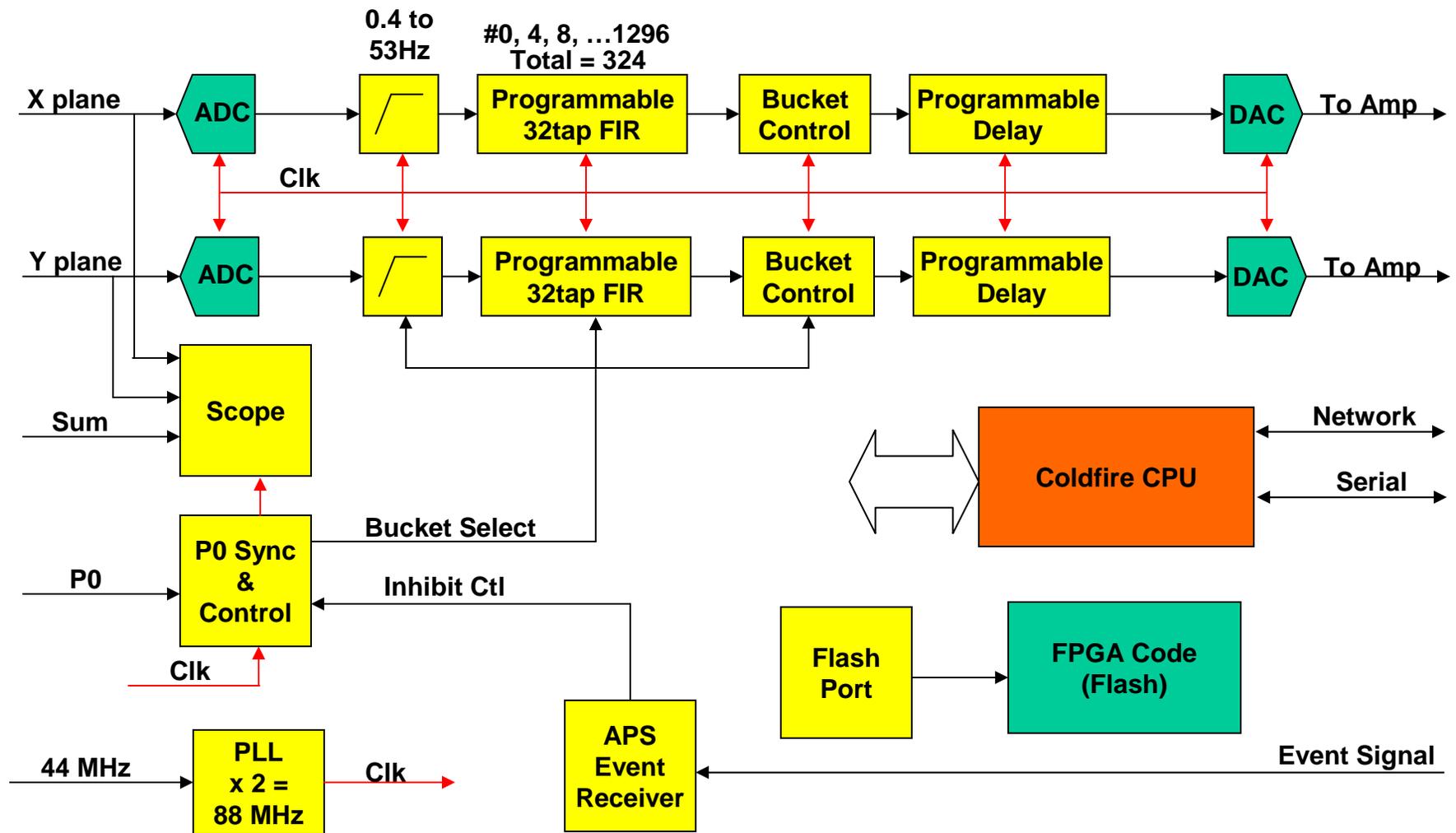
Hardware

- Altera Stratix II DSP Kit
 - Two 12 bit 125 MHz A/D
 - Two 14 bit 165 MHz D/A
 - 288 DSP 9-bit blocks (64 used)
 - 12 PLLs (2 used)
- Arcturus UCDIMM ColdFire 5282 CPU module (64 MHz)
 - 16 Megabyte SDRAM, 32-bit data path
 - 4 Mb Flash (App), 0.5 Mb Flash (bootstrap)
 - Ethernet, Serial
 - 5 Interrupt lines
- ColdFire transition module
- APS Event Receiver
- High Resolution A/D module (for Y-plane addition)
 - Two 14-bit 105 MHz A/D

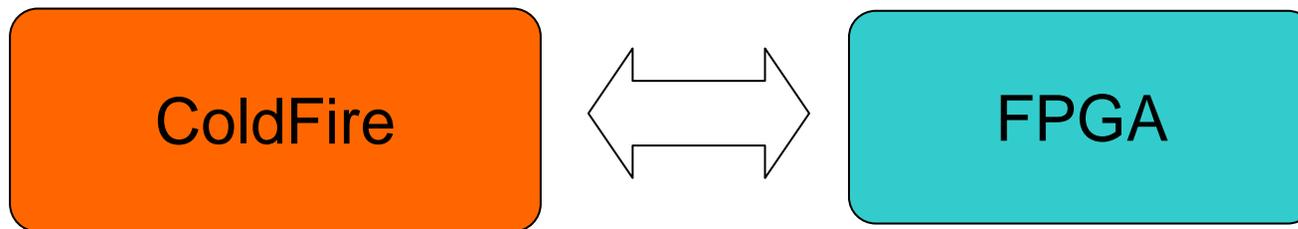
Hardware



Block Diagram of the P0 Feedback System



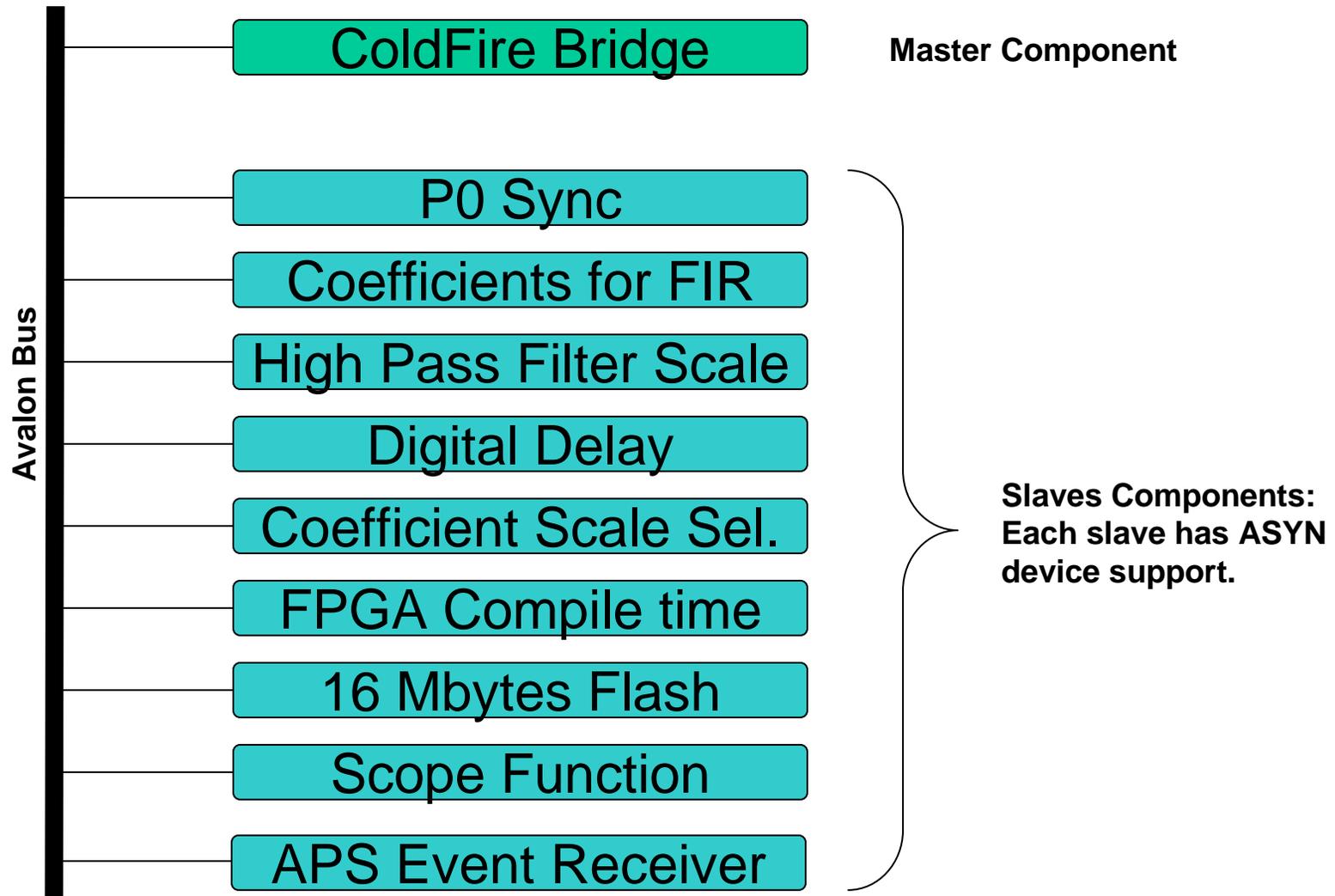
How to connect?



What will the device support look like?

Do you create a large memory/register map?

FPGA side, use Altera's Avalon Components for SOPC



FPGA

- Altera Quartus II 5.1 with SOPC builder
- SOPC creates a *system.h* file that defines all the devices on the Avalon Bus. This is used for all the ASYN & GTR device support.
- Multiple DSP cores
 - e.g. the P0 feedback computes $\sim 3 \times 10^9$ multiply-accumulate operations per second – Using less than 1/4 of the available multiplier (DSP) blocks.
 - This will double to $\sim 6 \times 10^9$ once the Y plane is added. More than half of the DSP blocks will be available.
- Originally designed for a single bunch, P0
 - but, the FPGA performs the algorithm in parallel, so the ‘P0 feedback’ can also be ‘P0, P4, P8, P1296’ feedback. (324)

IOC side: Device Support

- RTEMS 4.7
- EPICS R3.14.8.2
- VME like (devLib)
 - devReadProbe, etc.
- asynDriver: Asynchronous Driver Support
 - FPGA components
 - *asynInt32 – ai, ao, bo, longin, longout, mbbiDirect*
 - *asynInt32Array – waveform*
 - *asynFloat64Array – waveform*
 - *asynOctet - stringin*
- GTR: Generic Transient Recorder
 - For the Oscilloscope functions in the FPGA.
- Minimal device support when adding more FPGA components of the same type. (system.h)

Difficulties

- Mostly with the FPGA tools
 - Altera's SOPC builder
- Problem with spurious interrupts.
- Made ASYN more difficult than it was
 - no record types defined

Conclusion....

- Using Altera's Avalon bus reduced the FPGA development time. Simply drop in a new component and SOPC will automatically add it to the system. Components can be reused.
- Altera's Development Board eliminated the need to lay out a complex printed circuit board.
- ASYN and GTR greatly simplify device support.
 - This is really the way to go.
- The Coldfire CPU can be easily integrated with an FPGA.
- Only difference between VxWorks and RTEMS is how they are configured and how they download EPICS.
- In all, the tools from both EPICS and Altera helped produce a project ahead of schedule.