VME64x CR/CSR handling

- Introduction

- (non-existence of) support (in vxWorks)

- Discussion

CR/CSR Specification

- Configuration ROM/Control and Status Register, defined in VME64, additions in VME64x

- Address space with its own address modifier (0x2f)

- Module address in this space geographically addressed

- Each module has 512 kB, not all of it needs to be implemented

CR/CSR Specification

- Support for address space relocation (definable base)

- Module enable/disable

- Capabilities of the module (interrupt levels, support for special cycles)

- 8 "functions"; each function has its own addressing capabilities

- Module information (manufacturer, board ID, revision, serial number)

Status and Support

- All this is very nice (standardized interface for module-specific data, arranging of address space…) but
  - Very few modules on the market support this (I have seen only one example until now)
  - vxWorks BSPs (at least below version 6) have no idea of this
    - 4 master address windows, by default: A16, A24, A32, mailbox
  - How is it in RTEMS? I do not know
  - EPICS is not (coherently) using the 64x features

One example case

- The new Event System modules from Micro-Research ('200-series', a.k.a. Diamond timing) does implement CR/CSR specification.
  - How to handle this in the device support?
- Path of least resistance solution:
  - temporarily modify VME bridge (UniverseII) registers to give access to CR/CSR space, restore after configuration to original (J.Pietarinen)
  - Follow the same model as with Hytec cards: module address is calculated from the slot number (Diamond uses a lot of Hytec carrier boards)
  - Happens in startup script (would need rethinking if one wants hot-swap.)
  - No BSP modifications required; some assumptions of module number had/have to be corrected.

General issues

- What would be a good way to handle this kind of issues:
  - Try to forget about it (ask Micro-Research to 'downgrade' to fixed address mapping and hope that no new modules with CR/CSR appear)
    - If there is no OS support, it will be difficult to handle anyway
  - Attempt to figure out a concept, preferably with some kind of hardware abstraction layer
    - Are the 64x features ever going to be really used?