

8-Channel Power Supply Controller Performance and Functional Requirements

R. Hettel

- SPEAR 3 applications
- Corrector noise and stability requirements
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SPEAR 3 Applications

1. Fast orbit feedback:

54 H + 54 V orbit correctors

Corrector + supply bandwidth ~ 1 kHz

~ 200 Hz closed-loop bandwidth

\Rightarrow **2+ kHz feedback cycle rate**

Orbit kick resolution = ~ 0.01 μ rad (1.5 mrad FS)

\Rightarrow **7 ppm** \Rightarrow DAC ENOB = 17 bits or better

(APS upgraded to 18-bit; BESSY II to 20-bit)

2. Fast insertion device (ID) compensation (future):

ID modulation at ~ 100 Hz

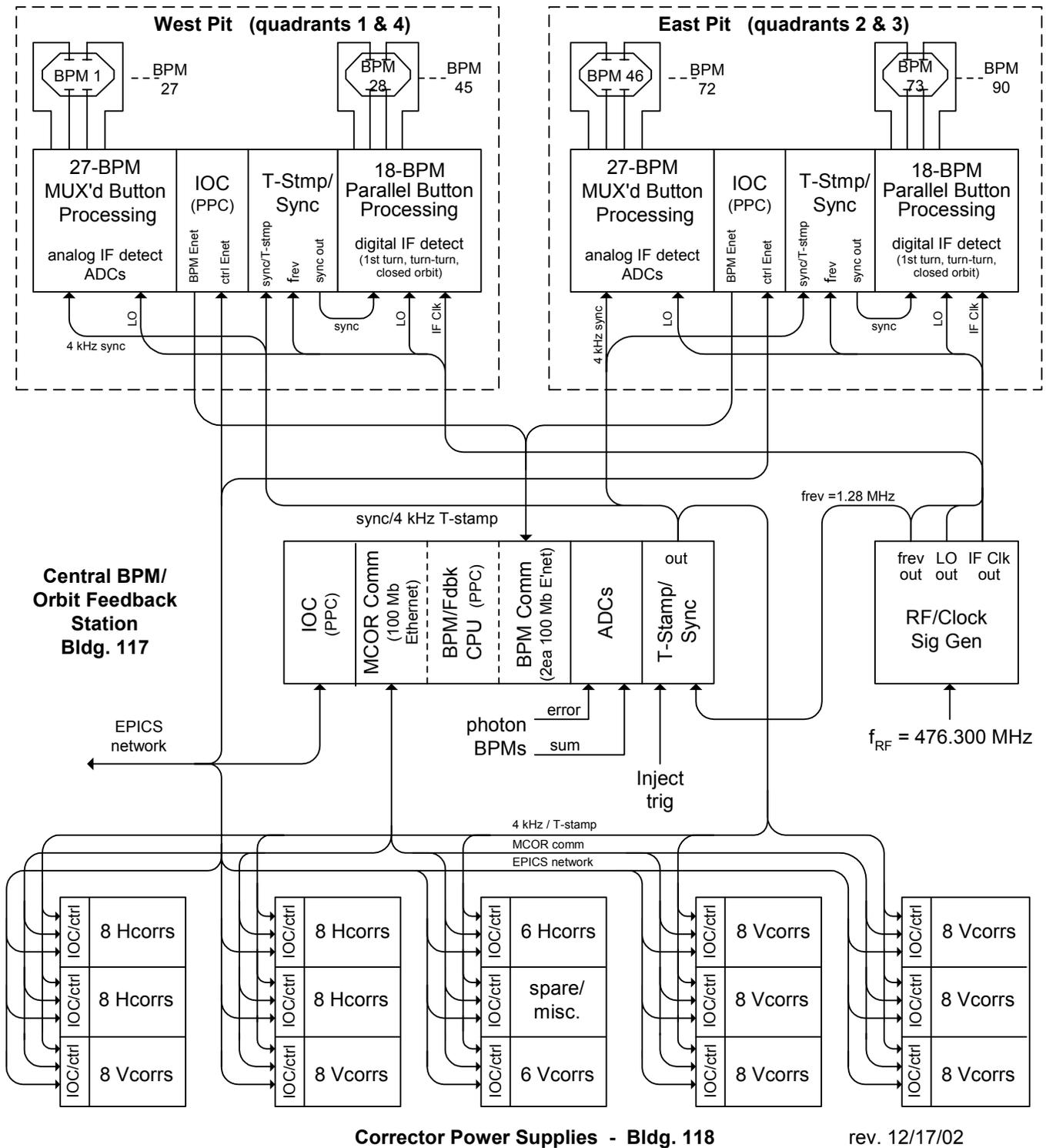
3. Stable DC orbit correction or ID compensation (no orbit feedback):

stability over 24 h, $\pm 2^\circ\text{C}$: **<0.005%** (14-bit equiv.)

With external supply current transducers, slow regulation via controller CPU:

stability over 24 h, $\pm 2^\circ\text{C}$: **<0.0015%** (16-bit equiv.)

SPEAR 3 BPM and Orbit Control System



Corrector Noise and Stability Requirements

1. Orbit stability specs:

$$\Delta y < 0.05 \sigma_y \quad (= 1.5 \mu\text{m rms at IDs})$$

$$\Delta y' < 0.05 \sigma_{y'} \quad (= 0.75 \mu\text{rad rms for 100-per undulator})$$

Stability over period T:

$$\text{data integration time } (\mu\text{secs}) < T < \text{hours } (\sim 24 \text{ h})$$

2. Orbit noise power spectral density:

$$\langle \Delta y^2 \rangle = \int \text{PSD } df$$

$$\Delta y (\text{peak}) = 3-5 \times \Delta y_{\text{rms}}$$

3. Orbit noise tolerances:

Orbit disturbance caused by DC kick θ_i from corrector i :

$$\Delta y(s) = \theta_i \frac{\sqrt{\beta_i \beta_s}}{2 \sin \pi \nu} \cos(|\varphi_i - \varphi_s| - \pi \nu)$$

Assume $\beta_i = 8$ m, $\beta_s = 5$ m, $\nu = 5.23$:

$$\Delta y_i(s, \text{max}) = 4.8 \theta_i \quad (\text{peak around ring})$$

$$\Delta y_i(s, \text{rms}) = 3.4 \theta_i \quad (\text{rms around ring})$$

For **uncorrelated** ensemble of N correctors ($N = 54$):

$$\Delta y_{\text{tot}}(s, \text{rms}) = 3.4 \sqrt{N} \theta_i (\text{rms}) = 25 \theta_i (\text{rms})$$

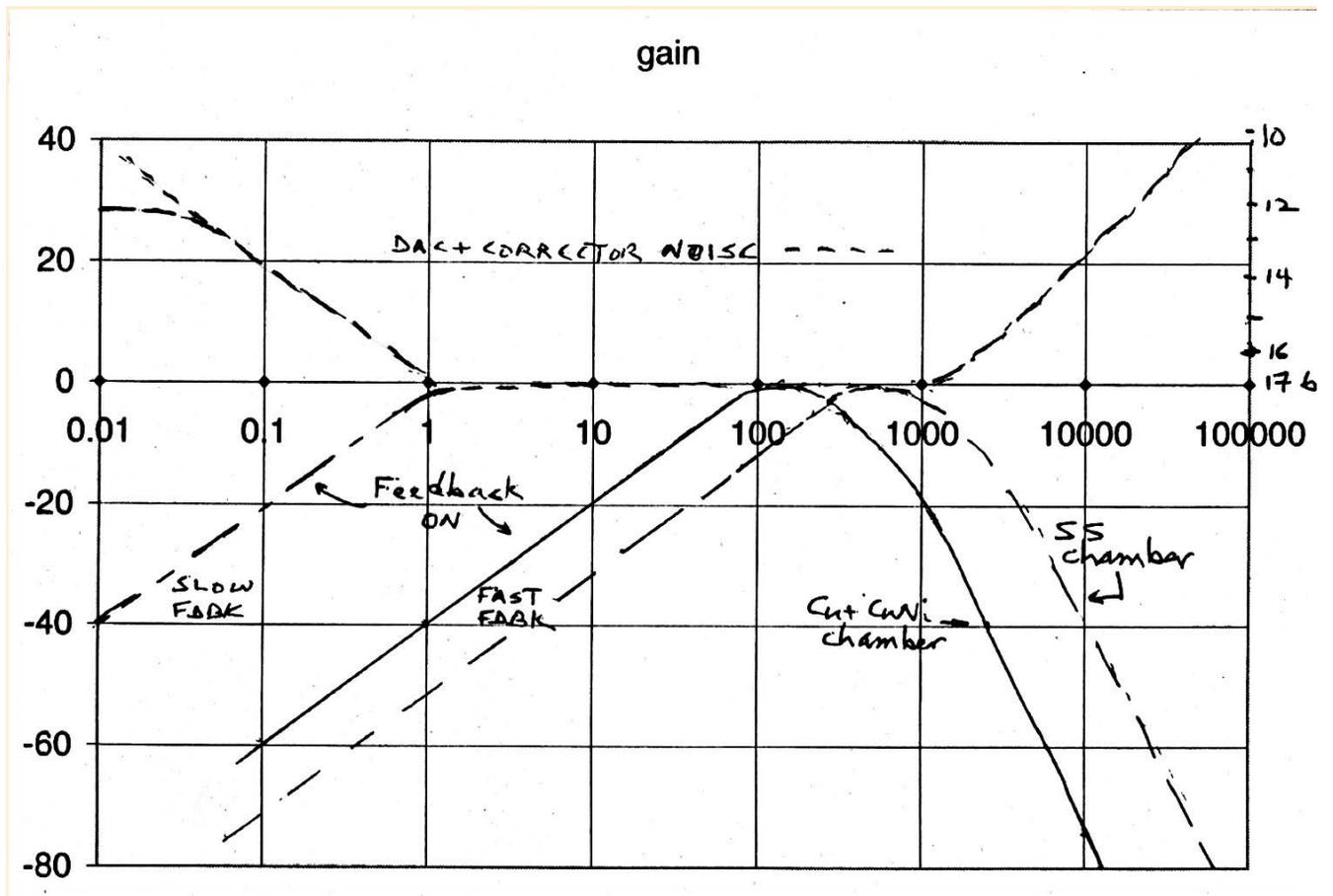
Limit noise contribution from correctors to **~10%** of total noise budget ----> limit $\Delta y_{\text{tot}}(s, \text{rms})$ from correctors to **<1%** of vert beam size ($0.3 \mu\text{m rms}$) with **feedback on**:

$$\Rightarrow \theta_i (\text{rms noise}) < 0.3 \mu\text{m} / 25 = \sim \mathbf{0.01 \mu\text{rad rms}}$$

$$\theta_i (\text{noise}) / \theta_{\text{Vcorr}} (\text{FS}) = \sim .01 / 1500 = \mathbf{7 \text{ ppm}}$$

Includes: - high freq filtering from vac chamber + magnets
- low freq noise attenuation by feedback

NOTE: - Feedback adds noise in bandwidth \geq cycle freq
- $\Delta y (\text{peak}) = 3\text{-}5 \times \Delta y_{\text{rms}}$



$$0.01 \mu\text{rad (rms)} = \left(\int_{0}^{0.1} \text{PSD} df + \int_{0.1}^{1} \text{PSD} df + \int_{1}^{10} \text{PSD} df + \int_{10}^{1\text{k}} \text{PSD} df + \int_{1\text{k}}^{10\text{k}} \text{PSD} df \right)^{1/2}$$

Conclude:

total noise in 0.001 Hz - 10 kHz BW = **< 10 ppm** per corrector
 stability over 24 h, $\pm 2^{\circ}\text{C}$: **< 0.005%** (open-loop)
 absolute accuracy: **< 0.1%**

PS Controller Functional Requirements

1. Control of 1-8 power supplies (selectable)
2. 100 Mb Ethernet control LAN
3. 4 ks/s DAC setpoint update rate for 8 supplies (20-bit)
4. Provision for external sync of DAC update
5. 4 ks/s readback of 3 ADC channels + status word for each of 8 supplies to buffer memory in PSC CPU
6. Readback data time stamping
7. Programmable readback filtering/decimation by PSC CPU
8. ADC and DAC calibration functions
9. Interlock functions
10. Test mode
11. Hardware encoded crate address through backplane
12. Setpoint data validity check by PSC CPU
13. DACs retain values if PSC CPU dies
14. History buffer for readback parameters
15. Provision for closed-loop supply regulation in PSC CPU (<1 Hz)
16. Provision for monitoring external high-performance current transducers (Ethernet)
17. Bulk supply control and monitoring
18. Front panel control and diagnostics (serial port and/or Ethernet)
- (19. Provision for analog control on supply modules?)

PS Controller Operating Modes

Phase 1:

Normal (open-loop)

Most recent network setpoint for each power supply passed directly to DAC within feedback cycle period (external sync input provided to synchronize multiple PSCs); digitally filtered network readback packet and signal history buffers updated at programmed rates.

Set-up

Normal operation halted; set-up parameters for specified PSC downloaded in one cycle; parameter readback packet updated; parameters can be read in "Setup Parameter Readback" mode.

Calibration

PSC executes automatic calibration routines to determine DAC and ADC gain and offset parameters for each of 8 power supply channels (interleaved with normal operation if possible); gain and offset info can be read back in "Calibration Readback" mode.

Test

To be defined.

Phase 2:

Closed-loop / I_{mon}

Most recent network setpoint for each power supply passed to summing node of feedback loop; digitized and digitally filtered readback from I_{mon1} subtracted from network setpoint and error signal passed through digital PID filter to DAC; digitally filtered network readback packet and signal history buffers updated at programmed rates.

Closed-loop / V_{mon}

Most recent network setpoint for each power supply passed to summing node of feedback loop; digitized and digitally filtered ΔV readback (voltage across supply output load) subtracted from network setpoint and error signal passed through digital PID filter to DAC; digitally filtered network readback packet and history buffers updated at programmed rates.

Closed-loop / DAC ?

PS Controller Readback Modes

Phase 1:

Normal

Readback packet for specified PSC contains monitored analog signals and power supply summary fault status for each of 8 channels of specified PSC; digitized analog signals are filtered by Readback filter, whose properties are specified in the Set-up parameters.

Set-up parameters

Readback word contains PSC address and data block containing values of all set-up parameters for 8 channels of specified PSC.

Calibration

Readback word contains PSC address, ADC and DAC calibration factors for each of 8 channels.

Test

to be specified

Phase 2:

Normal / multicycle

Readback packet contains PSC address, most recent status of Bulk Supply and controller parameters, and a data block containing current and voltage readbacks from each of 8 power supply channels for last N update cycles, where N is selectable between 1 and 16; current and voltage readback data are taken from the top N history buffer memory locations; other parameters are taken from the Readback filter.

History buffer - under consideration (multicycle mode may suffice)

Readback word contains PSC address, channel address, parameter identifier (read 1 parameter at a time), buffer block number (1-16), time stamp and data block containing up to 250 recorded values for the specified parameter stored in the specified history buffer data block; 16 cycles needed to read out entire 4k history record for power supply current or voltage.

Basal Mode

Set DAC, read back Imon1 for each channel

Interlock functions

Bulk PS over-voltage, under-voltage, ground current
Crate and module temperatures

PS Controller Control and Readback Parameters (to be incorporated in communication protocol)

Control parameters:

- PSC address
- PS enable/disable
- PS reset
- Op mode
- Setpoint data
- Set-up data
- Readback mode
- Readback data spec
- PS MUX select
- other?

Set-up parameters:

- Readback filter coefficients
- Readback decimation factor
- PS crate temp intlk thresh
- # multicycle readback cycles
- PS closed-loop filter coeffs
- PS closed-loop filter clk select
- Number of daughter board readback averages
- Bulk PS on/off
- other?

(potentiometer settings (?):

- Bulk PS overvolt thresh
- Bulk PS undervolt thresh
- Bulk PS gnd fault thresh)

PS Controller Control and Readback Parameters - cont.

Readback parameters:

per PSC:

- PSC address
- Op mode
- Rdbk mode
- Bulk PS voltage
- Bulk PS gnd curr
- Crate temp
- Controller fault word
- Set-up parameters
- Record time stamp
- other?

per PS (8 each):

- PS chan address
- I_{mon1}
- I_{mon2}
- V_{mon1}
- V_{mon2}
- (ΔV ?)
- DAC
- Temp
- Fault word