

BSP100 Module

- The BSP100 has a C-sized VXI form factor, with integrated stand-alone Experimental Physics and Industrial Control System (EPICS) input/output controller (IOC), and an Altera Stratix II Field-Programmable Gate Array (FPGA), with eight 14-bit A/D converters, Analog Device AD6645 running at 88 MHz.

- The BSP100's FPGA has five major blocks:
 1. The APS timing system receiver provides timing synchronization of the embedded IOC, generates triggered signals used by triggered block.
 2. The acquisition control block provides control signals for the receivers and directs the acquired samples to the appropriate processing blocks.
 3. The preliminary processing block reads the ADC values, computes the turn-by-turn average, and sends it to several other blocks for processing.
 4. The continuous signal processing block filters and linearizes the turn-by-turn average and forwards the appropriate values to the fast feedback and orbit control system.
 5. The triggered processing block provides data acquisition used for machine studies or post mortem analysis.

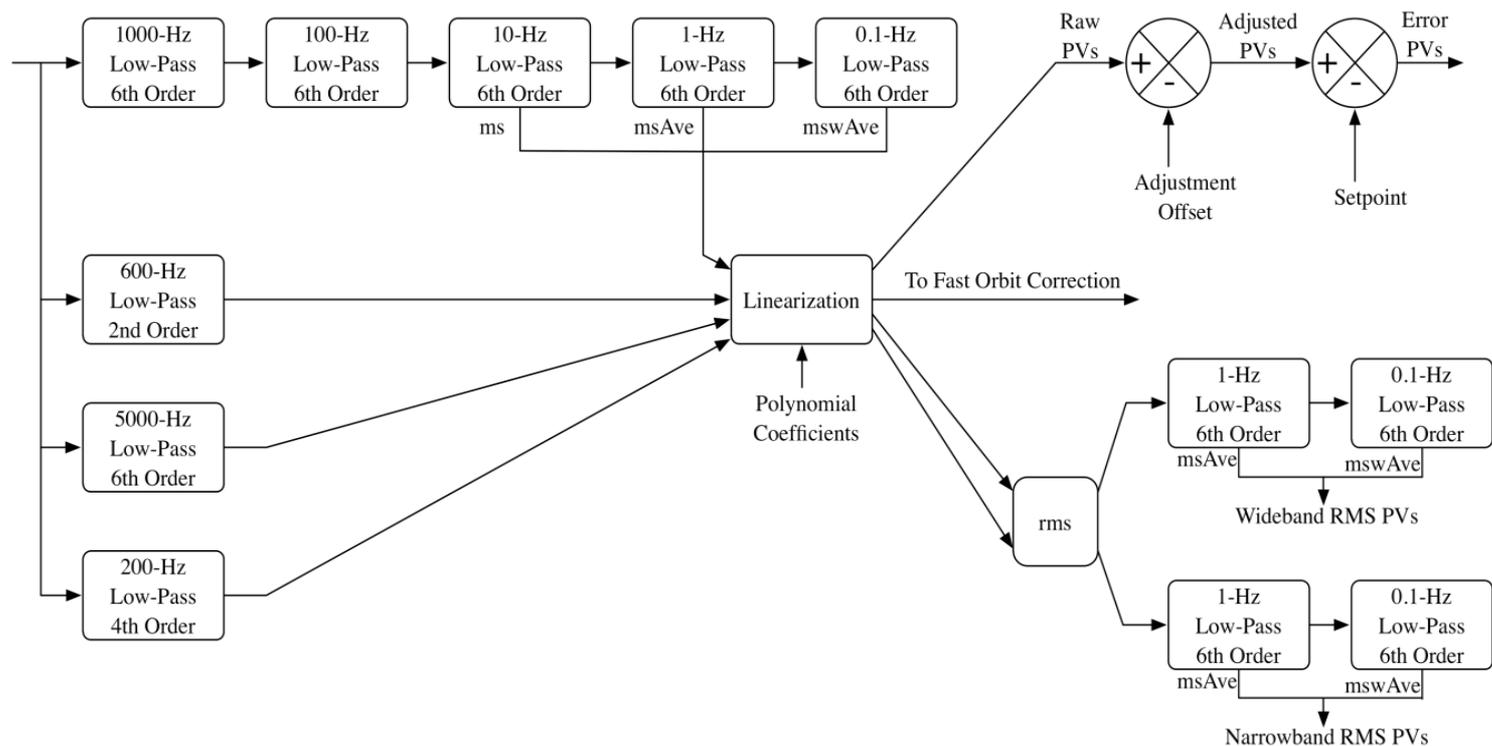


BSP100 cont'd

➤ BSP100 features:

- ❖ One second (262144 samples) turn-by-turn beam history for post mortem analysis
- ❖ Virtual digital oscilloscope (4096 samples @ 88 MHz)
- ❖ 100 Mb/sec serial link to RTFB system
- ❖ Demonstrated noise floor $< 10 \text{ nm} / \sqrt{\text{Hz}}$

BSP100 Continuous Signal Processing Block Diagram



Courtesy of E. Norum