# Workshop on Next-generation Fast Orbit Feedback Systems for Storage Rings

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**Design Process for APS FOFB System Upgrade**
9 May 2013

# Vivado High-Level Synthesis

- Algorithms: C or C++ or System C
- Testbench
- Synthesis
- Export
  - PCORE
  - SYSGEN
- Summary

# C or C++ or System C Algorithm

Vivado HLS - controllaw_prj (D:\DataPool_HLS\controllaw\controllaw_prj)

File Edit Project Solution Window Help

Debug Synthesis Analysis

Explorer

- controllaw_prj
  - Includes
  - Source
    - controllaw_hls.c
    - controllaw_hls.h
  - Test Bench
  - solution1
  - solution2
  - **solution3**
    - constraints
      - directives.tcl
      - script.tcl
    - csim
      - build
      - report
    - impl
      - pcores
      - report
      - sysgen
      - verilog
      - vhdl
    - sim
      - autowrap
      - report
      - systemc
      - tv
      - wrapc
      - wrapc_pc
    - syn
      - report
      - systemc
      - verilog
      - vhdl

*controllaw_hls.c

```
70
71 void err_calc( float bpm_in[SC_SIZE][BPM_SIZE], float sp_in[SC_SIZE][BPM_SIZE], float err[SC_SIZE][BPM_SIZE], fl
72 {
73 int i,j;
74 int r,c;
75 float bpm[SC_SIZE][BPM_SIZE];
76 float sp[SC_SIZE][BPM_SIZE];
77 float rinv[SC_SIZE][BPM_SIZE];
78
79 BPM_ERR_CALC_OUTER_LOOP:
80     for (i = 0; i < BPMS_ACTIVE ; i=i+1) {
81         BPM_ERR_CALC_INNER_LOOP:
82         for (j = 0; j < SC_SIZE ; j=j+4) {
83
84             bpm[j+0][i] = bpm_in[j+0][i];
85             bpm[j+1][i] = bpm_in[j+1][i];
86             bpm[j+2][i] = bpm_in[j+2][i];
87             bpm[j+3][i] = bpm_in[j+3][i];
88
89             sp[j+0][i] = sp_in[j+0][i];
90             sp[j+1][i] = sp_in[j+1][i];
91             sp[j+2][i] = sp_in[j+2][i];
92             sp[j+3][i] = sp_in[j+3][i];
93
94             rinv[j+0][i] = rinv_in[j+0][i];
95             rinv[j+1][i] = rinv_in[j+1][i];
96             rinv[j+2][i] = rinv_in[j+2][i];
97             rinv[j+3][i] = rinv_in[j+3][i];
98
99             err[j+0][i] = bpm[j+0][i] - sp[j+0][i];
100            err[j+1][i] = bpm[j+1][i] - sp[j+1][i];
101            err[j+2][i] = bpm[j+2][i] - sp[j+2][i];
102            err[j+3][i] = bpm[j+3][i] - sp[j+3][i];
103
104            acc[j+0] += err[j+0][i] * rinv[j+0][i];
105            acc[j+1] += err[j+1][i] * rinv[j+1][i];
```

Console Errors Warnings

Outline Directive

- controllaw_hls.h
- read_data(float[][], float[][], int) : void
- write_bpm_data(float[][], float[][], int
- write_cor_data(float[], float[], int) : vo
- zero_acc(float[]) : void
- err_calc(float[][], float[][], float[][], flo
- controllaw_hls(float[][], float[][], float

Vivado HLS - controllaw_prj (D:\DataPool_HLS\controllaw_test\controllaw_prj)

File Edit Project Solution Window Help

Debug Synthesis

Explorer

- controllaw_prj
  - Includes
  - Source
    - controllaw_hls.c
    - controllaw_hls.h
  - Test Bench
    - controllaw_hls_test.c
    - tb_data
      - bpm_err.dat
      - bpm_input.dat
      - bpm_results.dat
      - setpt_input.dat
  - solution1
  - solution2
  - **solution3**
    - constraints
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      - script.tcl
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      - report
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controllaw_hls.h controllaw_hls.c controllaw_hls_test.c

```
1 #ifndef __CONTROLLAW_HLS_H__
2 #define __CONTROLLAW_HLS_H__
3
4 #include <stdio.h>
5 #include <stdlib.h>
6 #include <math.h>
7
8 #define BPM_NUM  160
9 #define BPM_SIZE 500
10 #define SC_SIZE  4
11
12 #define BPM_RAND_OFFSET 51287
13 #define BPM_RAND_RANGE 16384
14
15 #define SETPT_RAND_OFFSET 56003
16 #define SETPT_RAND_RANGE 16384
17
18 #define RINV_RAND_OFFSET 38
19 #define RINV_RAND_RANGE  84
20
21 float BPM_IN[SC_SIZE][BPM_SIZE];
22 float SET_PT[SC_SIZE][BPM_SIZE];
23 float RINV[SC_SIZE][BPM_SIZE];
24
25 float BPM_ERR[SC_SIZE][BPM_SIZE];
26 float COR_ERR[SC_SIZE];
27
28 int BPM_ACTIVE;
```

- Floating Point Algorithm
  - Single Precision
- Header File

# Testbench

Vivado HLS - controllaw_prj (D:\DataPool_HLS\controllaw_test\controllaw_prj)

File Edit Project Solution Window Help

Debug | Synthesis | Analysis

Explorer

- controllaw_prj
  - Includes
  - Source
  - Test Bench
    - controllaw_hls_test.c
  - tb_data
  - solution1
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  - **solution3**
    - constraints
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      - script.tcl
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      - pcores
      - report
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      - verilog
      - vhdl
    - sim
      - autowrap
      - report
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      - wrapc
      - wrapc_pc
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      - report
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      - verilog
      - vhdl

controllaw_hls_test.c

```c
119
120     // Call the function to operate on the data
121     controllaw_hls(inBPM, inSETPT, inRINV, BPM_ERR, COR_ERR, BPMS_ACTIVE);
122
123     fp=fopen("tb_data/bpm_results.dat","w");
124     for (j=0;j<BPMS_ACTIVE;j++) {
125         for (i = 0; i < SC_SIZE; i++) {
126             u[i]=( BPM_ERR[i][j]);
127             fprintf(fp, "%f\t", u[i]);
128         }
129     fprintf(fp, "\n");
130     }
131     fclose(fp);
132
133     for (i = 0; i < SC_SIZE; i++) {
134         for (j=0;j<BPMS_ACTIVE;j++) {
135           if ( outBPM_ERR[i][j] != BPM_ERR[i][j]){
136             printf("Incorrect BPM output on sample %i,%i: \tExpected %f, \tReceived %f \n", i, j, outBPM_ERR[i]
137             retval_BPM = 1;
138              }
139         }
140     }
141
142     if (retval_BPM != 0) {
143         printf("BPM Test failed  !!!\n");
144         retval=1;
145     } else {
146         printf("BPM Test passed !\n");
147     }
```

Outline | Directive

- controllaw_hls.h
- main() : int

Console | Errors | Warnings

```
<terminated> controllaw_prj.Debug [C/C++ Application] D:\DataPool_HLS\control
BPM Test passed !
COR Test passed !
```

Vivado HLS - controllaw_prj (D:\DataPool_HLS\controllaw_test\controllaw_prj)

File Edit Project Solution Window Help

Debug | Synthesis

Explorer

- controllaw_prj
  - Includes
  - Source
    - controllaw_hls.c
    - controllaw_hls.h
  - Test Bench
    - controllaw_hls_test.c
    - tb_data
      - bpm_err.dat
      - bpm_input.dat
      - bpm_results.dat
      - setpt_input.dat
  - solution1
  - solution2
  - **solution3**
    - constraints
      - directives.tcl
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    - csim
      - build
      - report
    - impl
      - pcores
      - report
      - sysgen
      - verilog

controllaw_hls.h | controllaw_hls.c | controllaw_hls_test.c

```c
23  float outBPM_ERR[SC_SIZE][BPM_SIZE];
24  float outCOR_ERR[SC_SIZE];
25  FILE        *fp;
26
27  // Assign number of active BPMs
28  BPMS_ACTIVE = BPM_NUM;
29
30  // Create files of random data
31    fp=fopen("tb_data/bpm_input.dat","w");
32    for (j=0;j<BPMS_ACTIVE;j++) {
33        for (i = 0; i < SC_SIZE; i++) {
34            u[i]=( BPM_RAND_OFFSET + rand()/(RAND_MAX/BPM_RAND_RANGE));
35            v[i] = u[i]/1000.0;
36            fprintf(fp, "%f\t", v[i]);
37        }
38    fprintf(fp, "\n");
39    }
40    fclose(fp);
41
42    fp=fopen("tb_data/setpt_input.dat","w");
43    for (j=0;j<BPMS_ACTIVE;j++) {
44        for (i = 0; i < SC_SIZE; i++) {
45            u[i]=( SETPT_RAND_OFFSET + rand()/(RAND_MAX/SETPT_RAND_RANGE));
46            v[i] = u[i]/1000.0;
47            fprintf(fp, "%f\t", v[i]);
48        }
49    fprintf(fp, "\n");
50    }
```

- Generate Data for Comparison
- Compare Data
- Self Checking
- Return 0 on pass

# Synthesis

Vivado HLS - controllaw_prj (D:\DataPool_HLS\controllaw_test\controllaw_prj)

File Edit Project Solution Window Help

Debug | Synthesis

Explorer

- bpm_err.dat
- bpm_input.dat
- bpm_results.dat
- setpt_input.dat
- solution1
- solution2
- **solution3**
  - constraints
    - directives.tcl
    - script.tcl
  - csim
    - build
    - report
  - impl
    - pcores
    - report
      - verilog
      - vhdl
    - sysgen
    - verilog
    - vhdl
  - sim
    - autowrap
    - report
    - systemc
    - tv
    - wrapc
    - wrapc_pc
  - syn
    - report
      - controllaw_hls_csynth.rpt
      - err_calc_csynth.rpt
      - read_data_csynth.rpt
    - systemc
    - verilog
    - vhdl

controllaw_hls.h | controllaw_hls.c | controllaw_hls_test.c | **controllaw_hls_csynth.rpt**

**User Assignments**

| | |
|---|---|
| Product Family: | kintex7 |
| Part: | xc7k325tffg900-2 |
| Top Model name: | controllaw_hls |
| Target clock period (ns): | 10.00 |
| Clock uncertainty (ns): | 1.25 |

**Performance Estimates**

**Summary of timing analysis**

Estimated clock period (ns): 8.50

**Summary of overall latency (clock cycles)**

| | |
|---|---|
| Best-case latency: | 985 |
| Average-case latency: | 985 |
| Worst-case latency: | 985 |

**Summary of loop latency (clock cycles)**

WR_COR_Loop_Col

**Area Estimates**

**Summary**

| | BRAM_18K | DSP48E | FF | LUT | SLICE |
|---|---|---|---|---|---|
| Component | - | 19 | 2154 | 3018 | - |
| Expression | - | - | 0 | 107 | - |
| FIFO | - | - | - | - | - |
| Memory | 12 | - | 0 | 0 | - |
| Multiplexer | - | - | - | 72 | - |
| Register | - | - | 138 | - | - |
| ShiftMemory | - | - | - | - | - |
| Total | 12 | 19 | 2292 | 3197 | 0 |
| Available | 890 | 840 | 407600 | 203800 | 50950 |
| Utilization (%) | 1 | 2 | ~0 | 1 | 0 |

Console | Errors | Warnings | Man Page

Vivado HLS Console

Outline | Directive

- Report Version
- General Information
- User Assignments
- Performance Estimates
  - Summary of timing analysis
  - Summary of overall latency (clock cycles)
  - Summary of loop latency (clock cycles)
- Area Estimates
  - Summary
  - Details
  - Hierarchical Multiplexer Count
- Power Estimate
  - Summary
  - Hierarchical Register Count
- Interface Summary
  - Interfaces

- Set Clock
- Interface Modes
  - GUI
  - TCL
- Directives
  - Latency
  - Loops
  - Pipelining

# Export: PCORE

Vivado HLS - controllaw_prj (D:\DataPool_HLS\controllaw_test\controllaw_prj)

File Edit Project Solution Window Help

Debug | Synthesis

Explorer

- csim
  - build
  - report
- impl
  - pcores
    - controllaw_hls_top_v1_00_a
      - data
        - controllaw_hls_top_v2_1_0.bbd
        - controllaw_hls_top_v2_1_0.mpd
        - controllaw_hls_top_v2_1_0.pao
        - controllaw_hls_top_v2_1_0.tcl
      - doc
      - include
      - netlist
        - controllaw_hls_ap_faddfsub_2_full_dsp.ngc
        - controllaw_hls_ap_fmul_1_max_dsp.ngc
      - simhdl
      - synhdl
        - verilog
          - BPM_ERR_if.v
          - BPM_IN_if.v
          - controllaw_hls_ap_faddfsub_2_full_dsp.v
          - controllaw_hls_ap_faddfsub_2_full_dsp.x
          - controllaw_hls_ap_fmul_1_max_dsp.v
          - controllaw_hls_ap_fmul_1_max_dsp.xco
          - controllaw_hls_ap_rst_if.v
          - controllaw_hls_buf_bpm_in.v
          - controllaw_hls_faddfsub_32ns_32ns_32_
          - controllaw_hls_fmul_32ns_32ns_32_3_ma
          - controllaw_hls_top.v
          - controllaw_hls.v
          - COR_ERR_if.v

controllaw_hls_csynth.rpt | controllaw_hls_export.rpt

Report date: Sun May 5 03:41:59 CDT 2013

**Resource Usage**

| | VHDL | Verilog |
|---|---|---|
| SLICE | 562 | - |
| LUT | 1440 | - |
| FF | 1546 | - |
| DSP | 19 | - |
| BRAM | 12 | - |
| SRL | 0 | - |

**Final Timing**

| | VHDL | Verilog |
|---|---|---|
| CP required | 10.000 | - |
| CP achieved | 7.588 | - |

VHDL: Timing met

Outline | Directive

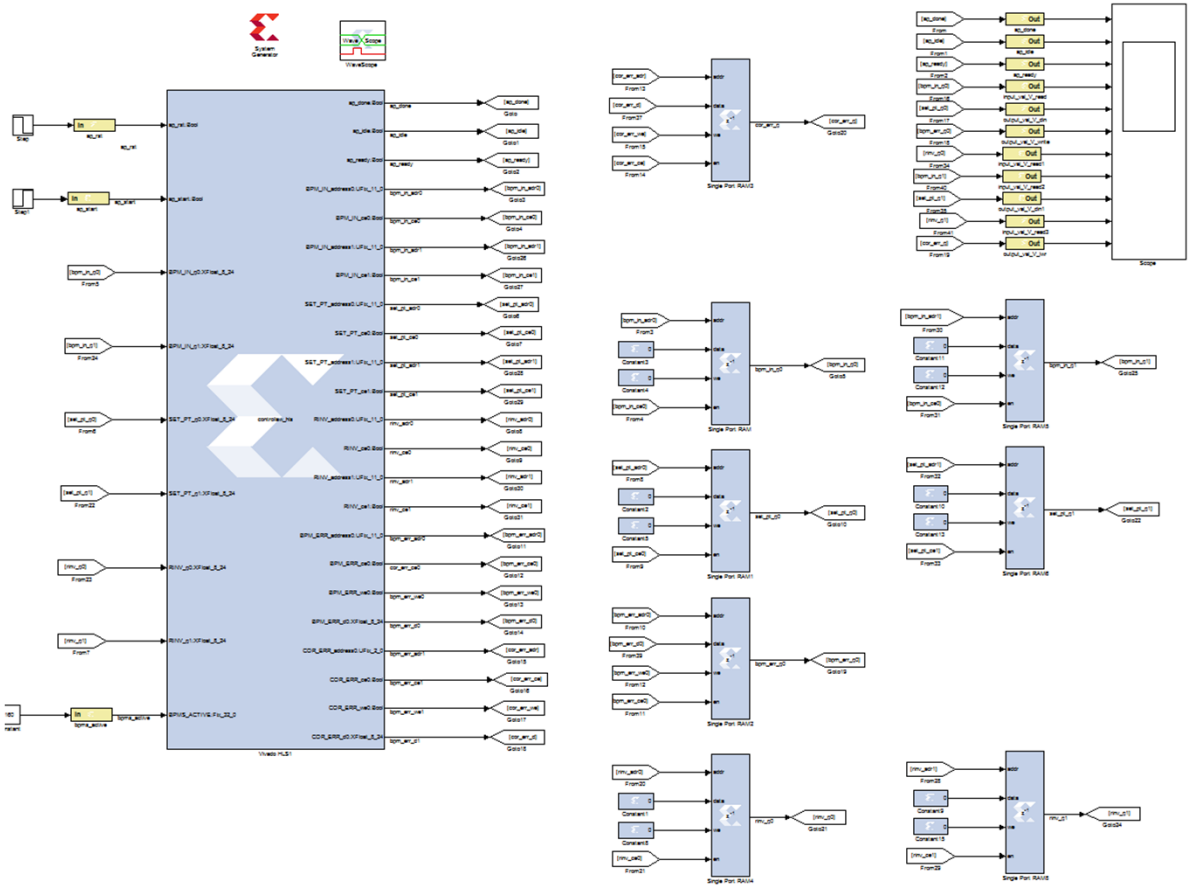
An outline is not available.

Console | Errors | Warnings | Man Page

Vivado HLS Console

```
DSP:            19
BRAM:           12
SRL:             0
#=== Final timing ===
CP required:    10.000
CP achieved:    7.588
Timing met
```

# Export: SYSGEN



- Earlier Version with 8 RAMs
- User Created Model
- DSP Wavescope

# Vivado High Level Synthesis Summary

- Test with Double Precision
- Test in routed design with hardware/software interaction

- Vivado HLS
  - C to RTL design
  - Testbench for validation
  - Measures latency
  - Resources Utilized
  - Export: PCORE and SYSGEN

- To learn more:
  - Vivado Design Suite Tutorial High Level Synthesis
    - Xilinx User Guide - UG902
  - C-based Design: High-level Synthesis With Vivado HLS
    - Xilinx Authorized Training Provider
  - *Floating-Point PID Controller Design with Vivado HLS and System Generation for DSP*
    - Xilinx Application Note - XAPP1163