Workshop on Next-generation Fast Orbit Feedback Systems for Storage Rings

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Design Process for APS FOFB System Upgrade
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Delay Spreadsheet

Libera GDX External Loopback TX_SOF to RX_SOF + Latency																			
	Fields	Packet Width		User Clocks	Clock	1st Packet	Latency	TX/RX	Hops	uS					Total		Ts (uS)	Percent	
Calculated	34	16		46	8.00E-09	3.68E-07	2.64E-07	1	1	0.63					0.63		44.25	1.43%	
Measured	34	16		52	8.00E-09	4.16E-07	2.64E-07	1	1	0.68					0.68		44.25	1.54%	
BPM Sample Period																			
Fs (Hz)															Delay (uS)	Sum (uS)	Ts (uS)	Percent	Selected Method
22600										44.25					44.25	44.25	44.25	100.00%	100.00%
TX/RX BSP-100 Taxi to RTFB DSC																			
	Fields	Packet Width	Bits	Encoded Bits	Clock	1st Packet	Latency	TX/RX	Hops	uS									
	51	8	408	1.25	1.00E-08	1.00E-07	5.00E-06	1.03922	1	5.30					5.30		44.25	11.98%	
	43	8	344	1.25	1.00E-08	1.00E-07	4.20E-06	1.04651	1	4.50					4.50	4.50	44.25	10.17%	10.17%
TX/RX with Taxi to SC																			
	Fields	Packet Width	Bits	Encoded Bits	Clock	1st Packet	Latency	TX/RX	Hops	uS	SC	Serial CRC	Delay	uS			Ts (uS)	Percent	
	41	16	656	1.25	1.00E-08	2.00E-07	8.00E-06	1.04878	1	8.60	10	16	1.60E-06	1.60	10.20		44.25	23.05%	
SC Fiber Delay																			
SC = 2*(1104meters + 210meters)/20										0.64					0.64	0.64	44.25	1.46%	1.46%
Power Supply Serial Interface																			
Format		Bits	SC Clk (uS)	uS		Measured (uS)		TX/RX									Ts (uS)	Percent	
Serial		18.00	1.60	28.80				1.05556							30.40		44.25	68.70%	
(31,16,3) BCH Code		31.00	0.05	1.55				1.03226							1.60	1.60	44.25	3.62%	
Serial		18.00				4.00									4.00	4.00	44.25	9.04%	9.04%
Fast Corrector: Regulator Response						120.00									120.00	120.00	44.25	271.20%	271.20%
Fast Corrector: Beam Response						138.30													
Fast Corrector: Beam - Regulator						18.30									18.30	18.30	44.25	41.36%	41.36%
TX/RX with Aurora to SC																			
Aurora				User Clocks	Clock	1st Packet	Latency	TX/RX	Hops	uS		Parallel CRC							
10b8b (32b)	40	1		61	5.00E-09	3.05E-07	1.95E-07	1	10	5.00	10	1	5.00E-08	0.05	5.05	5.05	44.25	11.41%	11.41%
10b8b (16b)	80	1		52	5.00E-09	2.60E-07	3.95E-07	1	10	6.55	10	1	5.00E-08	0.05	6.60		44.25	14.92%	
66b64b (64b)	20	1		52	5.00E-09	2.60E-07	9.50E-08	1	10	3.55	10	1	5.00E-08	0.05	3.60		44.25	8.14%	
RTFB DSC Algorithm																			
SC Error Calcuation: 1000 cycles at 5ns				Cycles	Clock		Latency			uS									
985 cycles				1000	5.00E-09		5.00E-06			5.00					5.00	5.00	44.25	11.30%	11.30%
TX/RX with Aurora around SR																			
Aurora				User Clocks	Clock	1st Packet	Latency	TX/RX	Hops	uS		ID Lookup							
66b64b (64b)	110	1		61	5.00E-09	3.05E-07	5.45E-07	1	21	17.85	21	4	4.20E-07	0.42	18.27	18.27	44.25	41.29%	41.29%
SR Fiber Delay																			
SR = 1104meters + 210meters										6.44					6.44	6.44	44.25	14.55%	14.55%
Sample Update Rate																228.05 us			511.78%
Effective Frequency																4.38 KHz			
Loop Bandwidth using Sampling Frequency Ratio					25											0.17539876 KHz			
Loop Bandwidth using Sampling Frequency Ratio					40											0.10962422 KHz			