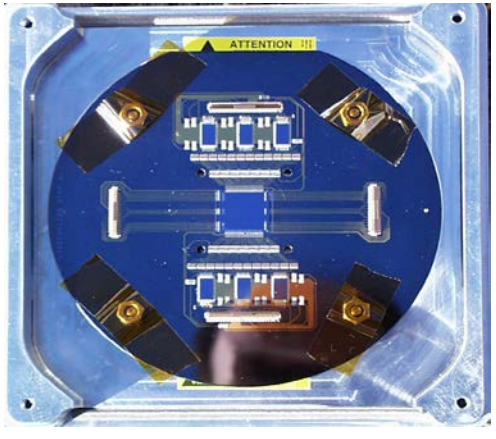
FCCD Project Status (Last updated on 3-3-2008)

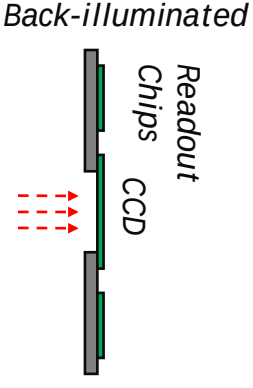
- Integration Milestones Completed by both LBNL and ANL
  - Initial test of 480 x 480 CCD using LBNL's leach control for CCD biases and ANL's Clock Modules for the clock signals

- Milestones Completed (LBNL)
  - Received fCRIC readout chips
  - Received Fast CCD Chips
  - Performed initial testing of fCRIC
  - Tested 4-port version (20x480) of Fast CCD

- Milestones Completed (ANL)
  - Built Interface, Data, and Clock Modules.
  - Created a GUI to control setup and configuration of electronics.
  - Read test data from a fCRIC

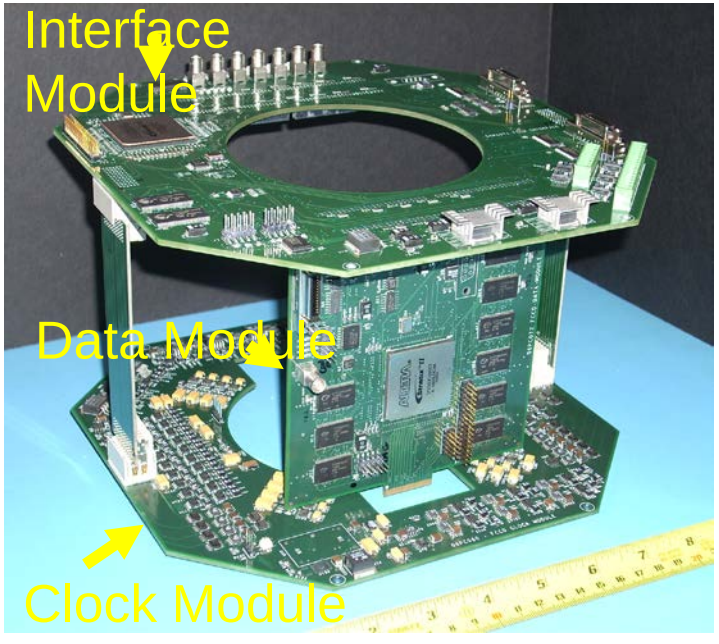
LBNL - CCD silicon assembly
P. Denes, Spring, 2007





3-mm thick x 6 inch Si substrate
Au metalization
Polyimide passivation
Processed at UC Berkeley MicroLab

ANL – Back End Electronics
J. Weizeorick, Spring, 2007



FCCD Project Status

- LBNL Future Milestones
  - Make detector assembly with CCDs and six fCRICs
  - Put assembly into vacuum housing and test cooling system

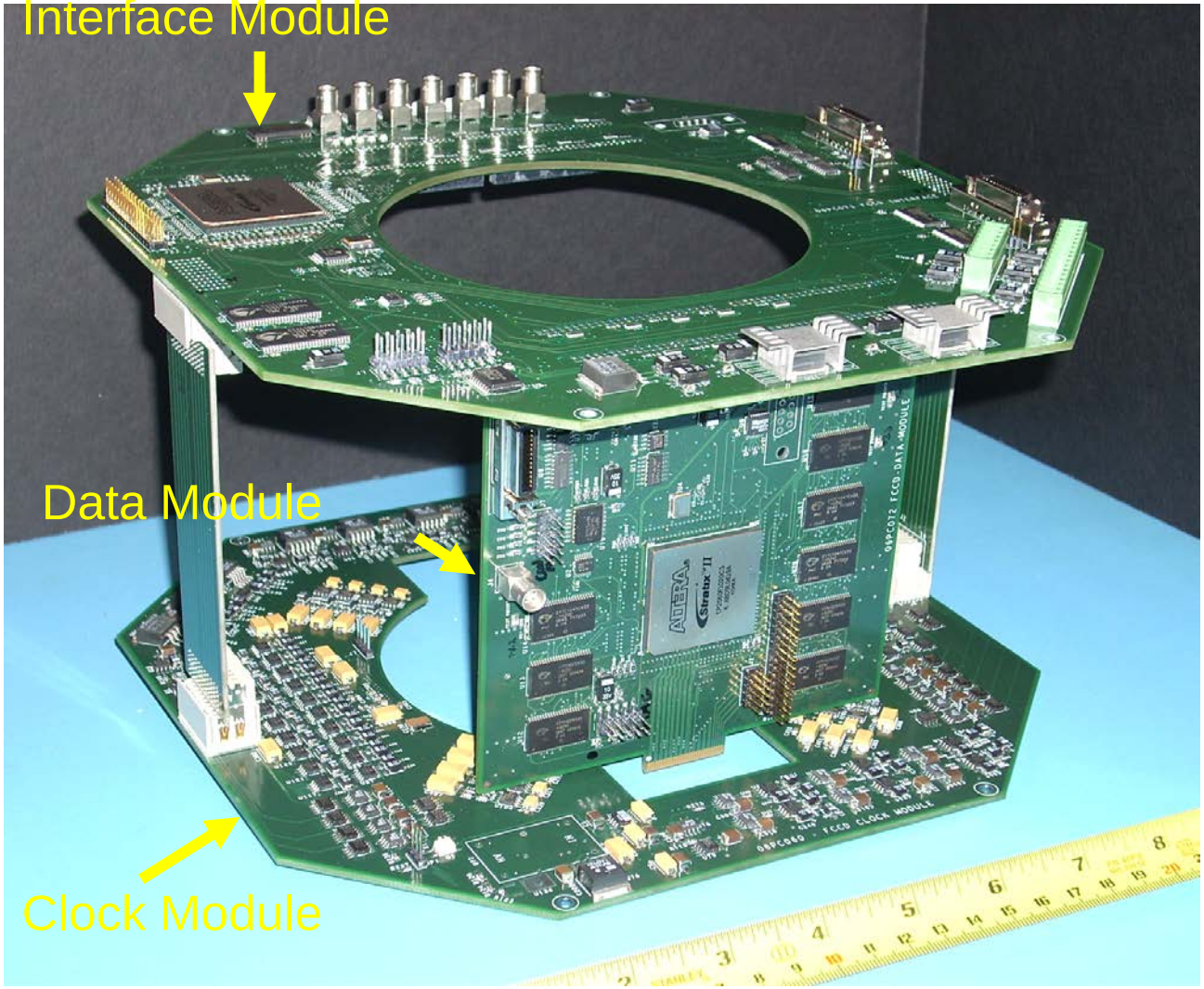
- ANL Future Milestones
  - Ship computer and power supply for the FCCD detector to LBNL
  - Improve GUI to make testing at LBNL faster and easier
  - Finish FPGA code for Interface and Data Module
    - *Program data module to receive data from 3 fCRICs*
    - *Program Interface Module to receive data from 2 Data modules*
    - *Implement Descrambling in data module*

- Combined Milestones
  - Integrate assembly with 480 x 480 CCD and six fCRICs.
  - Characterize FCCD Detector (first optically then with x-rays)
  - Test and build Interlock and Cooling system
  - Work with users to improve user interface
  - Complete documentation

FCCD Project Images

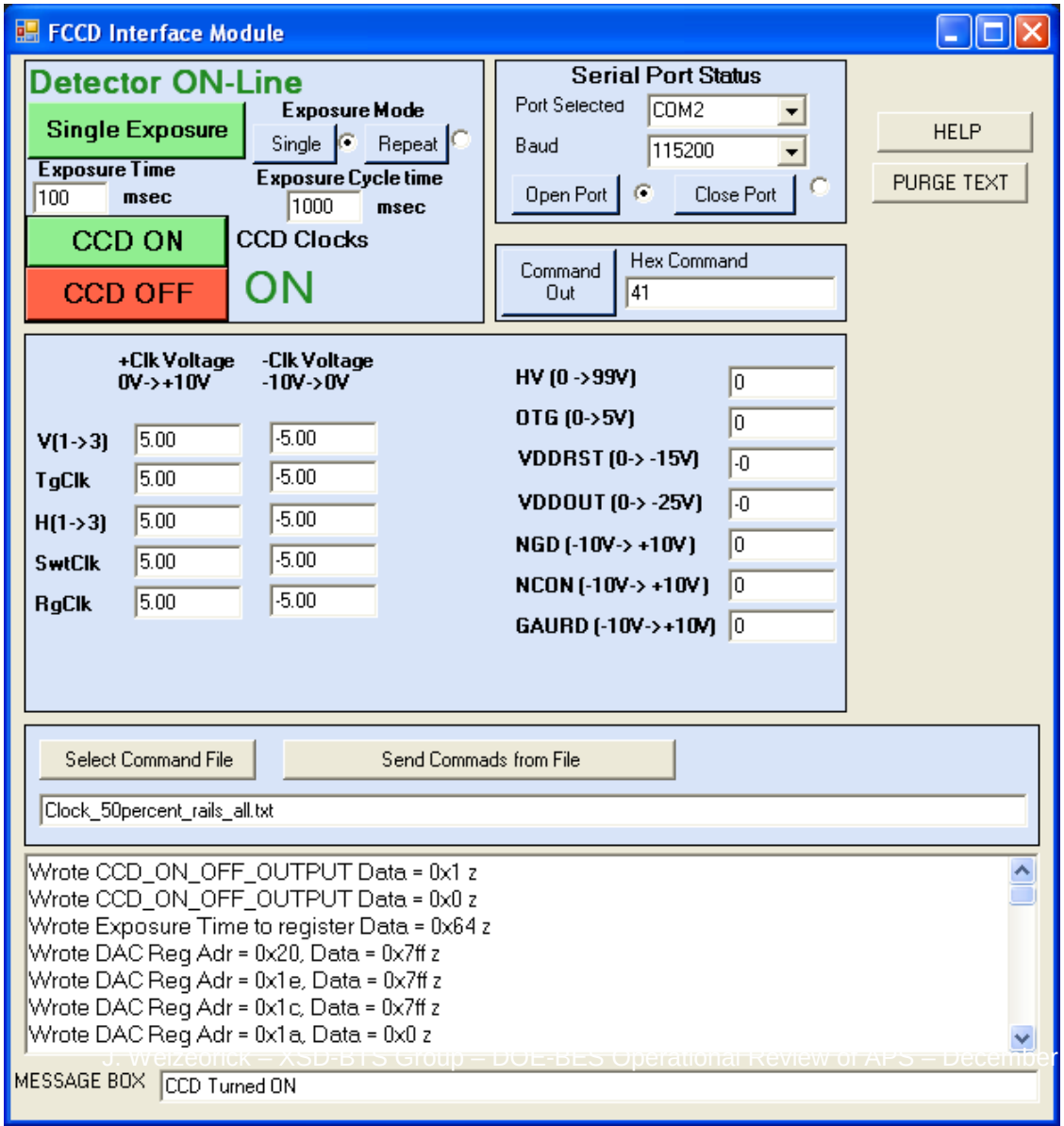
- ***APS/XSD-BTS Backend Electronics***

ANL – Back End Electronics
J. Weizeorick, Spring, 2007



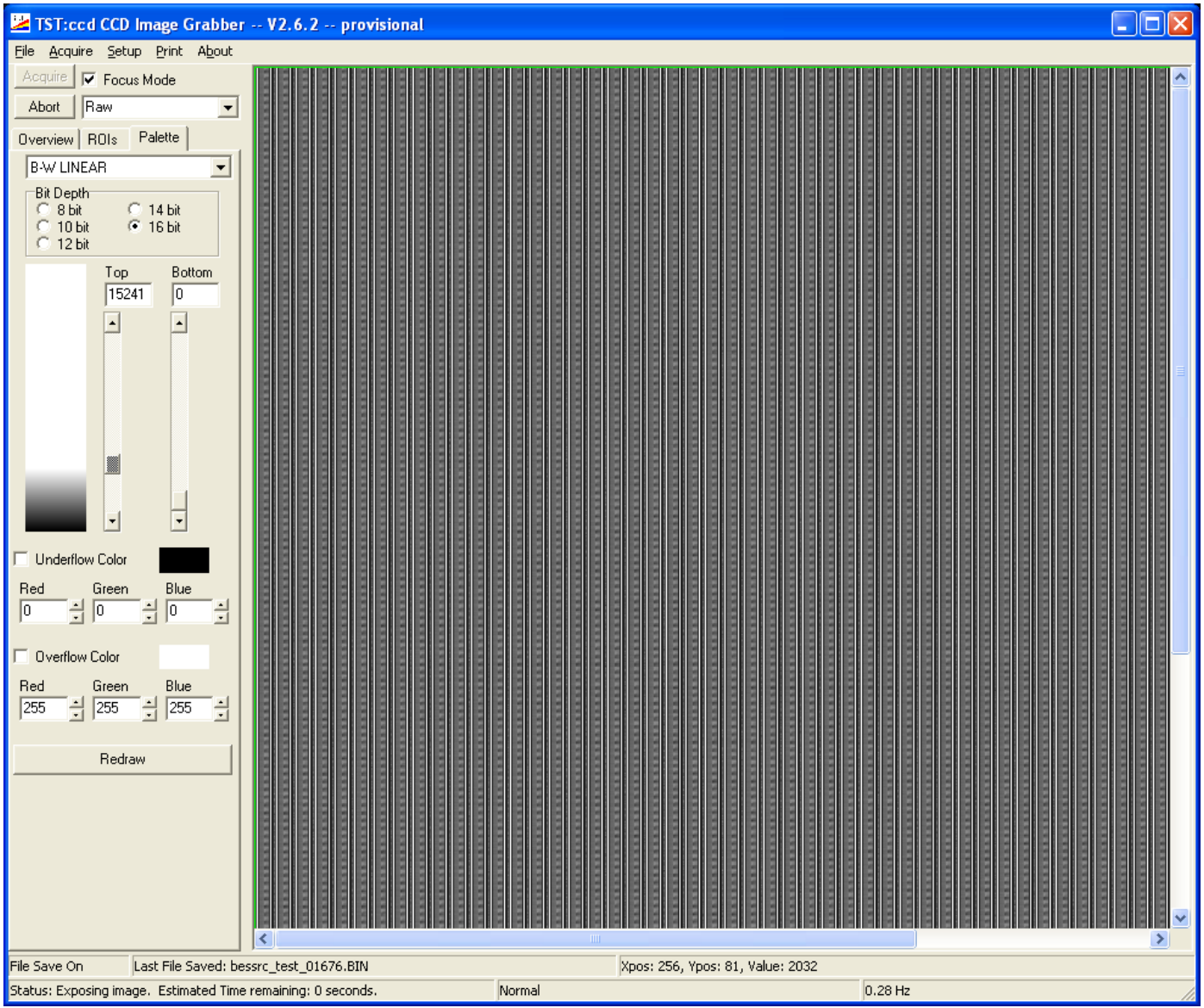
FCCD Project Images

APS/XSD-BTS – GUI to configure and control hardware



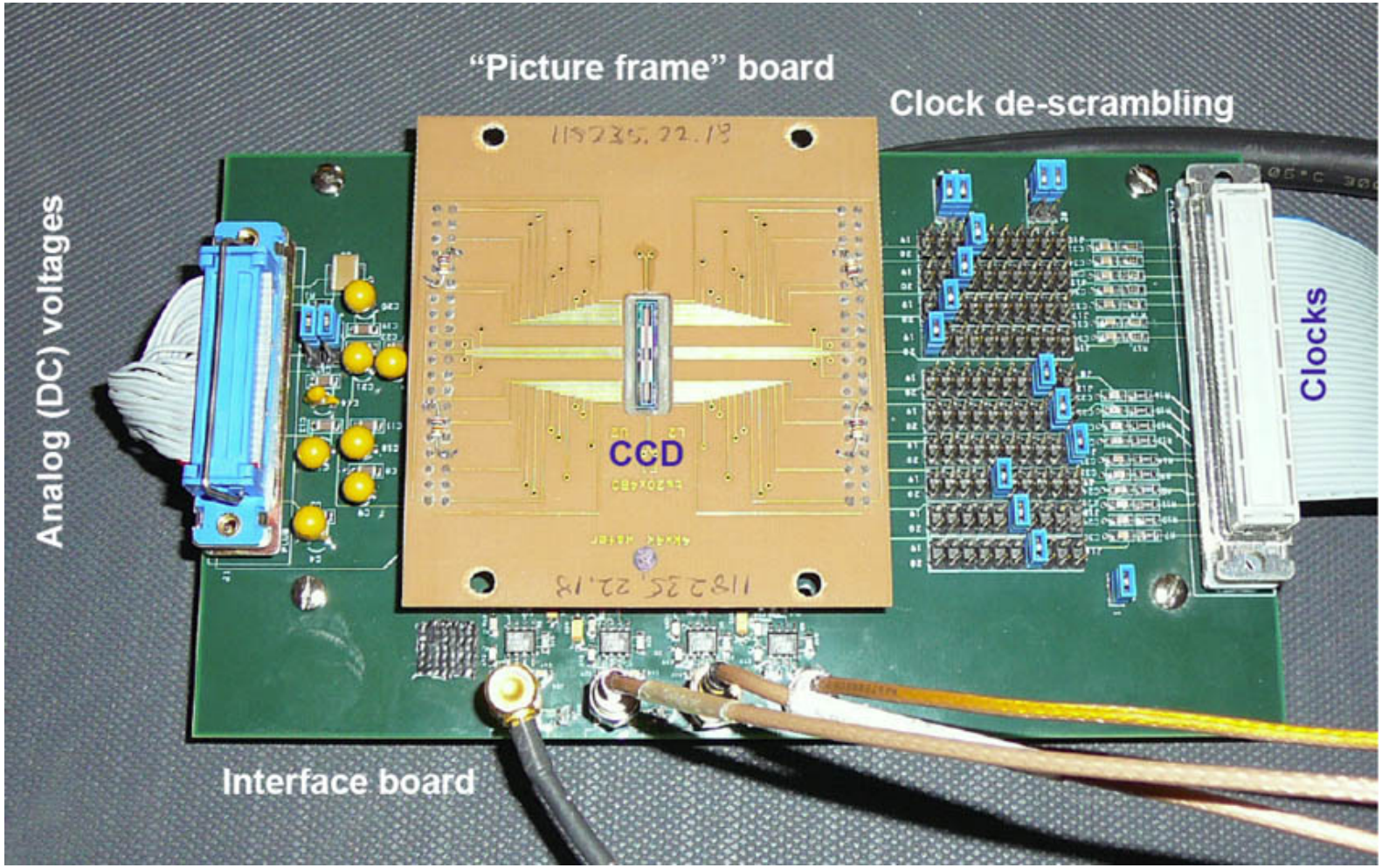
FCCD Project Images

APS/XSD-BTS – User Interface and Image Viewer



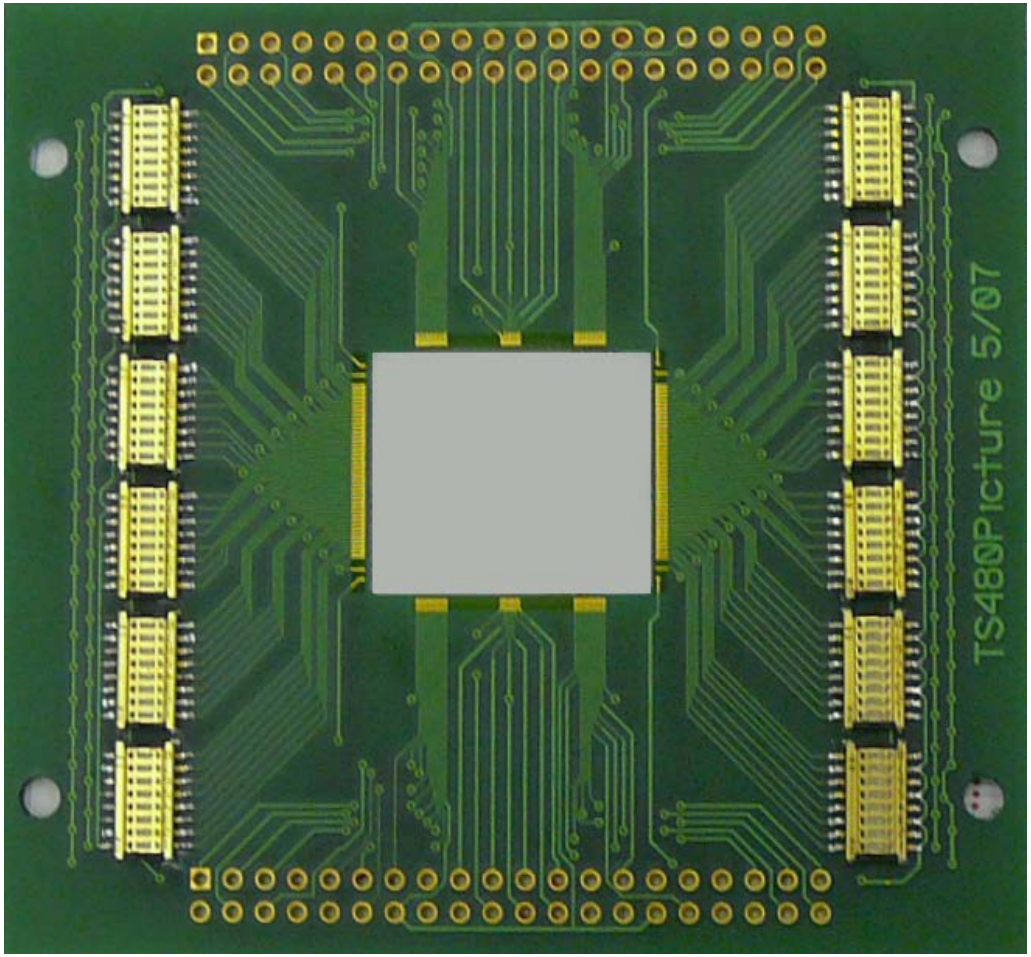
FCCD Project Images

LBNL – CCD Test Setup for 4-port version (20x480)



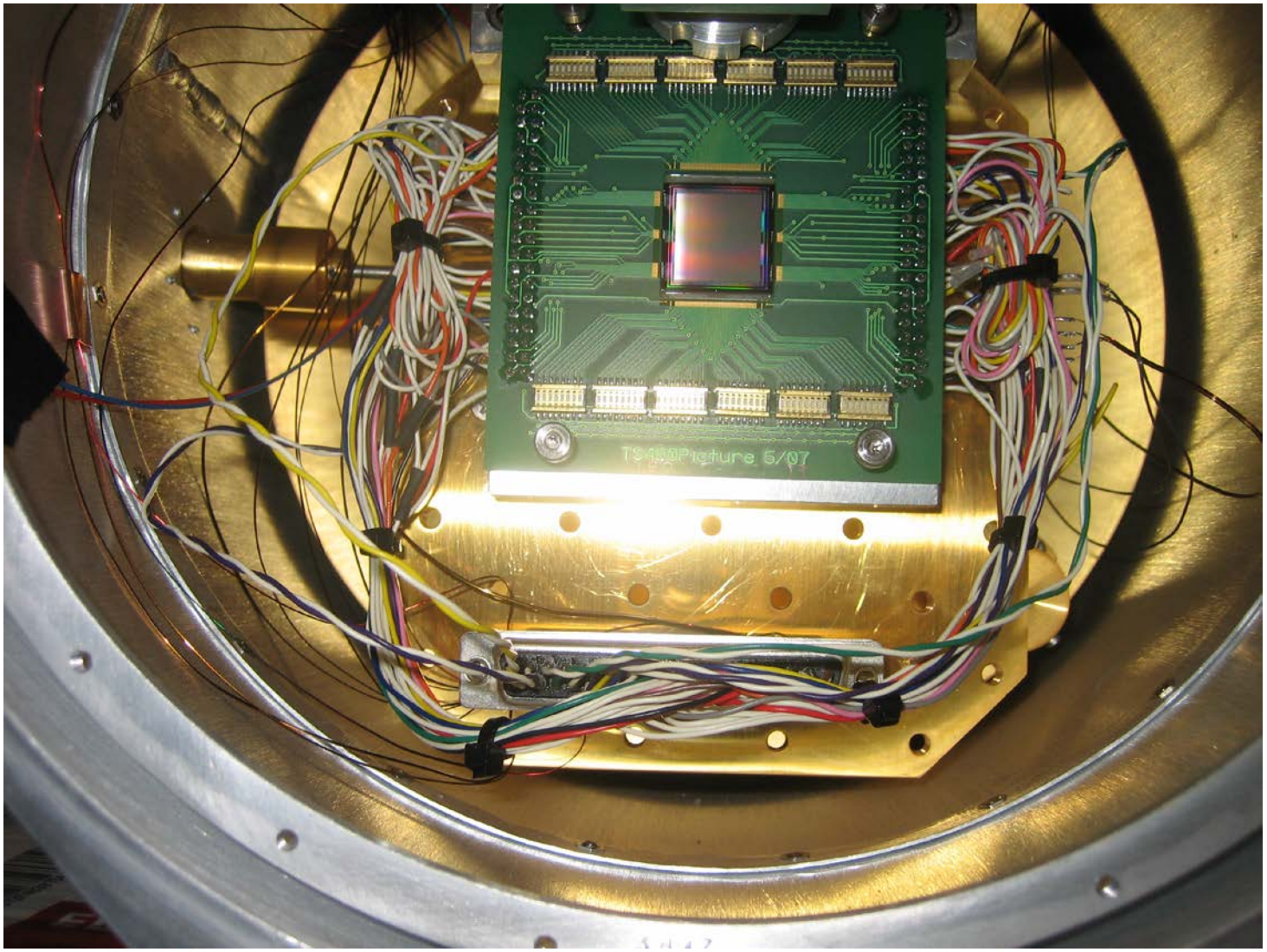
FCCD Project Images

LBNL - Picture frame board for 480 x 480, 96 port CCD (with 96 switches!)

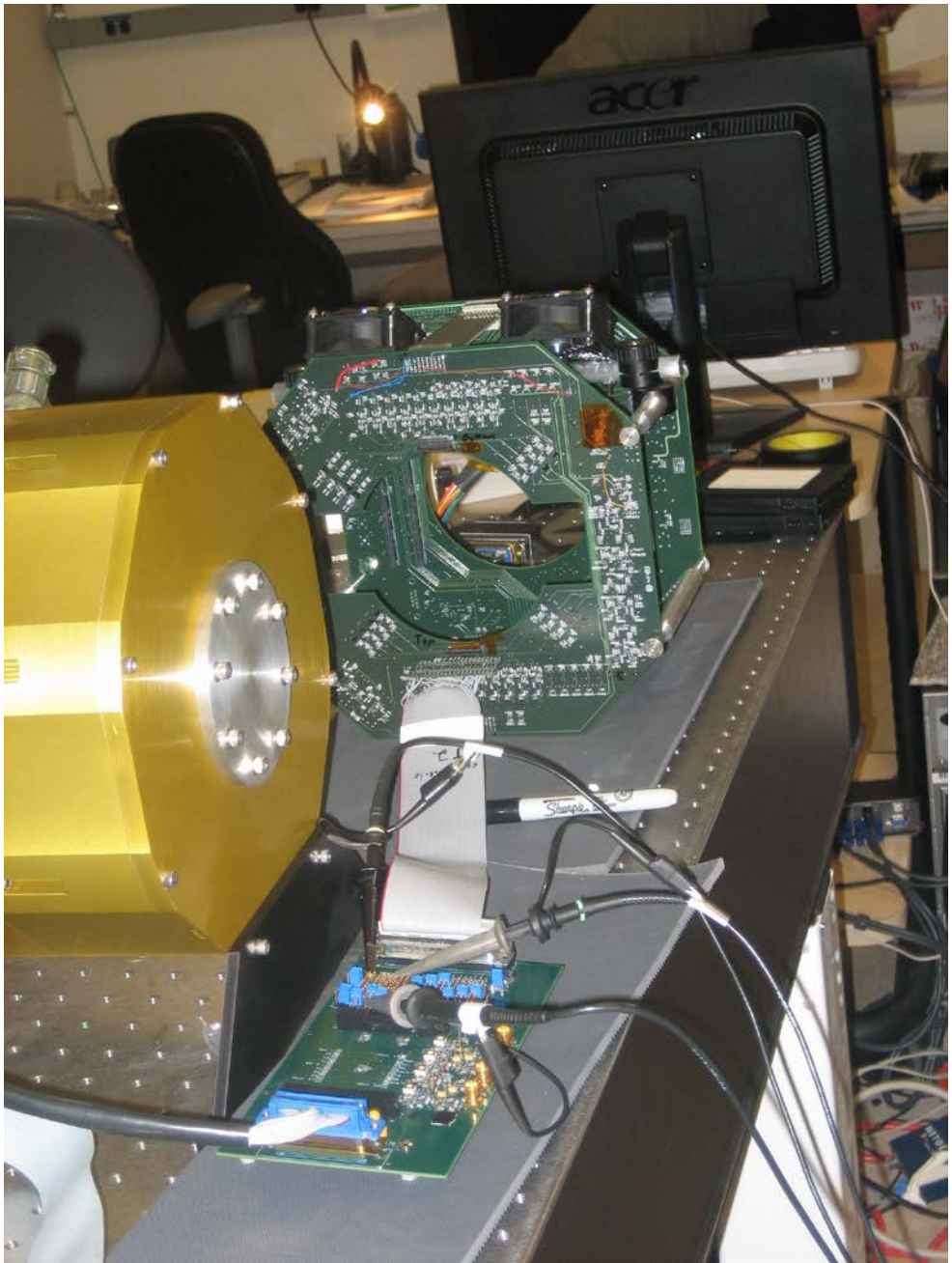


FCCD Project Images

Picture frame board for 480 x 480, 96 port CCD inside Nitrogen Dewar



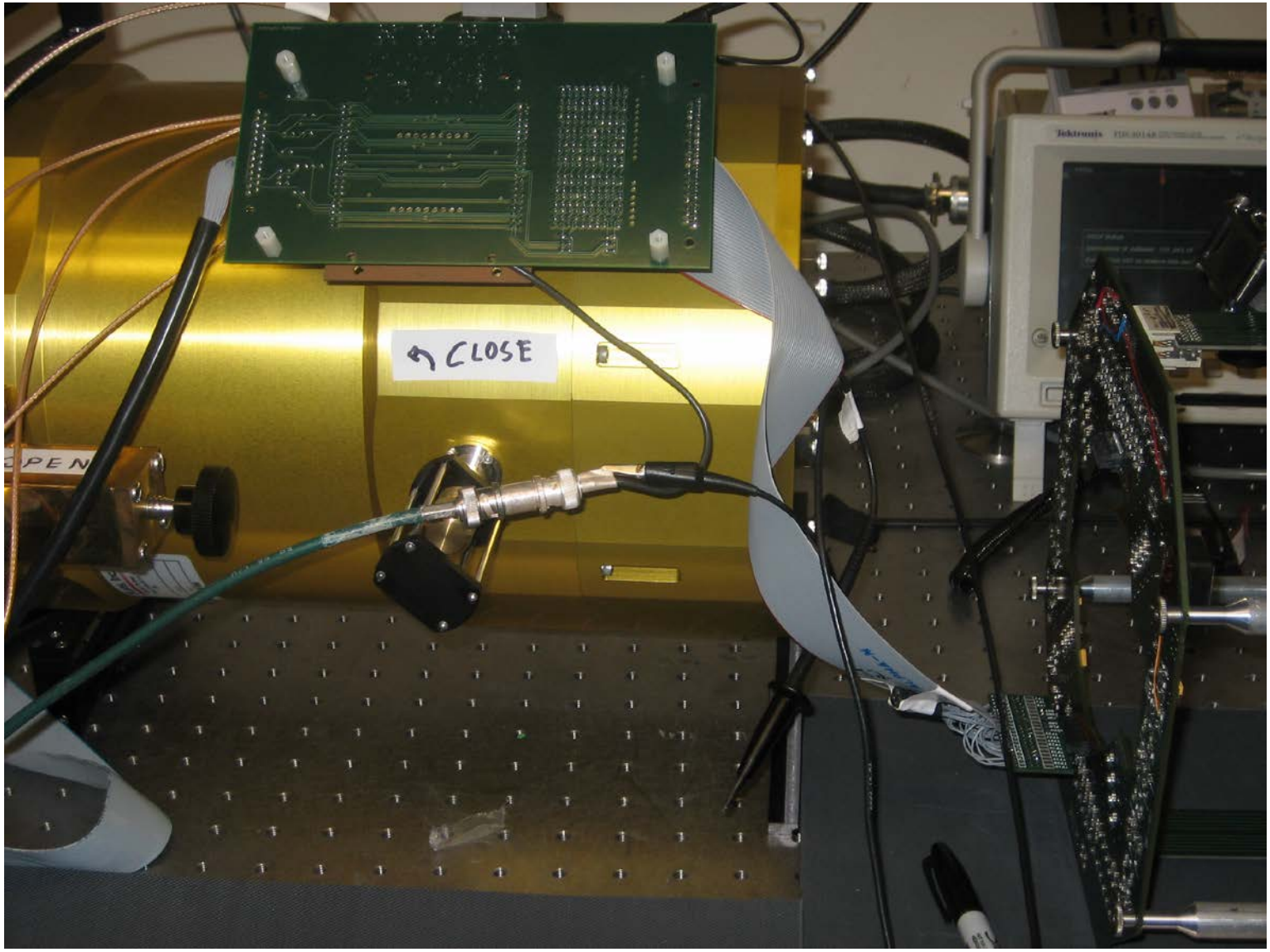
FCCD Project Images



Nitrogen Dewar Closed up, Clock Signals coming from ANL's Clock Module and Bias Voltages coming from Leach Controller

FCCD Project Images

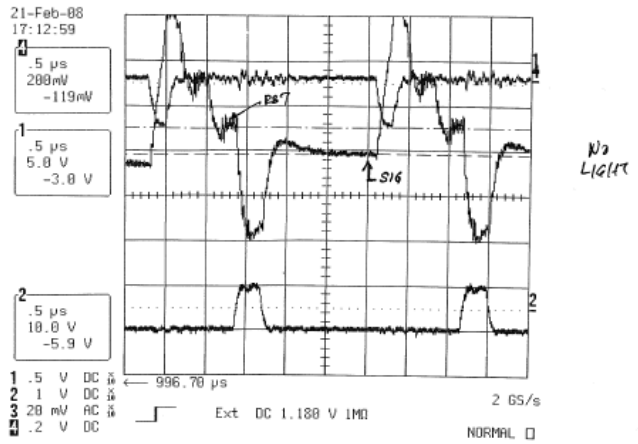
Signal board plug into Dewar. Ready to take Data with scope



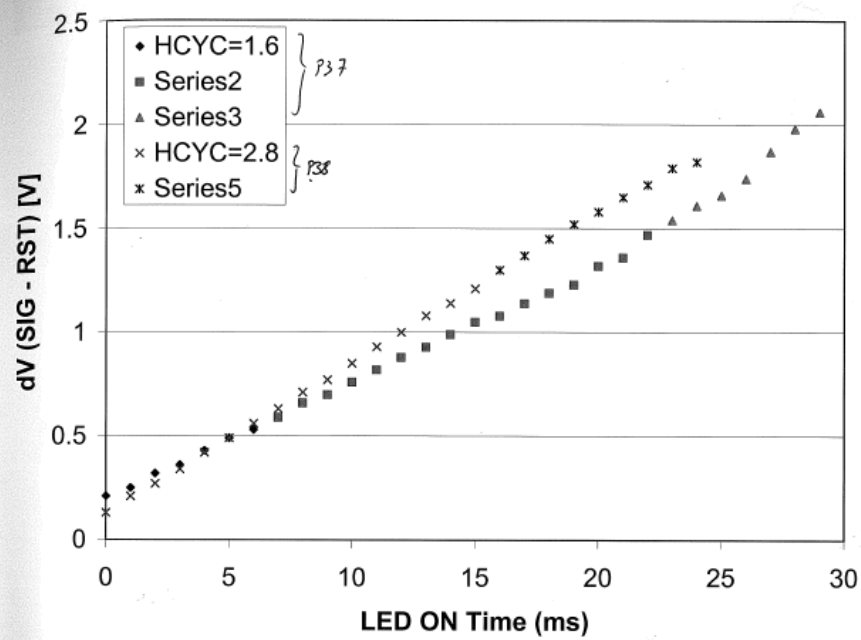
FCCD Project Images

First Light Measurements of 480 x 480 CCD

Recompiled FPGA on Interface Module again
Change Hcyc cycle from 1.6 µs to 2.8 µs
~~Tick~~ cycles per tick changed from 3 → 6
100nsec 175nsec



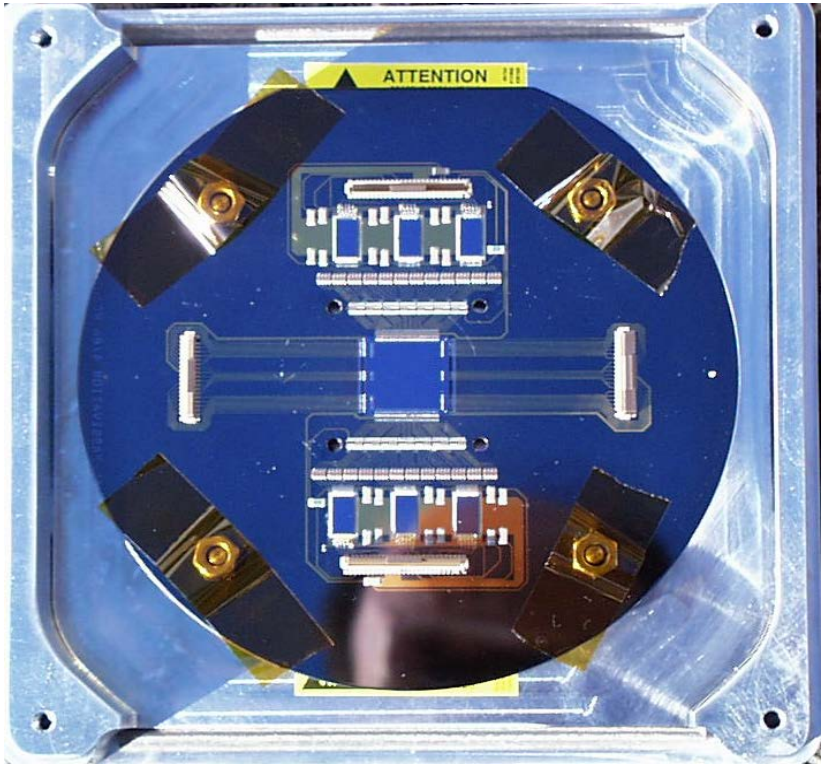
0	0.13	16	1.30	→ Change gain
1	0.21	17	1.37	→ 1.30 (New gain)
2	0.27	18	1.45	
3	0.34	19	1.52	
4	0.42	20	1.58	
5	0.49	21	1.65	
6	0.56	22	1.71	
7	0.63	23	1.79	
8	0.71	24	1.82	
9	0.77	25	1.	→ Sat.
10	0.85	26		
11	0.93	27		
12	1.00	28		
13	1.08	29		
14	1.14	30		
15	1.21			

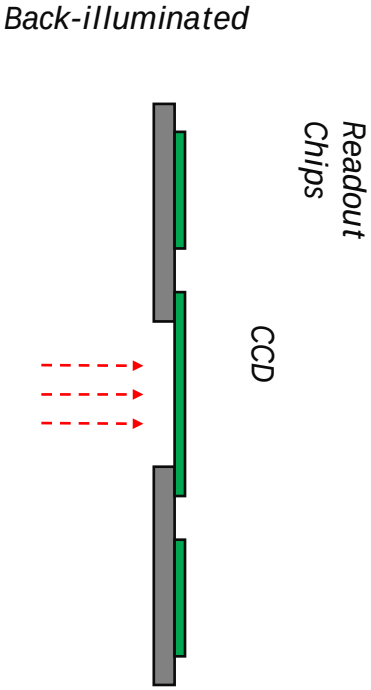


FCCD Project Images

LBNL Mechanical Test of Assembly with CCD and six fCRICs

LBNL - CCD silicon assembly
P. Denes, Spring, 2007





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