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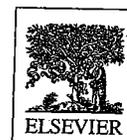
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by

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## Epitaxy — a new technology for fabrication of advanced silicon radiation detectors

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### Abstract

Twenty five years after the introduction of the planar process to the fabrication of silicon radiation detectors a new technology, which replaces the ion implantation doping by silicon epitaxy is presented. The power of this new technique is demonstrated by fabrication of silicon drift detectors (SDDs), whereby both the n-type and p-type implants are replaced by n-type and p-type epi-layers. The very first SDDs ever produced with this technique show energy resolutions of 150 eV for <sup>55</sup>Fe at −35 °C. The area of the detectors is 10 mm<sup>2</sup> and the thickness 300 μm. The high potential of epitaxy for future detectors with integrated complex electronics is described.

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### 1. Introduction—state of the art

About 30 years ago the planar process for the fabrication of high-quality radiation detectors was developed by J. Kemmer and first published by him in 1980 [1]. Since that time this technology has been successfully applied for the development and

fabrication of a great variety of silicon radiation detectors including simple pin-diodes, position sensitive detectors like strip detectors, pixel detectors and pn-CCDs [2] as well as for detectors showing high energy resolution for X-rays like silicon drift detectors (SDDs) [3].

The technology could be improved during this period to enable the integration of special FETs into the detectors [4] as realized for the pn-CCDs, the pixel detectors and the SDDs. Though introduction of the planar process was considered

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as a quantum step in detector fabrication, further improvements are possible, scarcely, it has reached its limits. It seems to be impossible, for instance, to make this technology compatible with modern techniques used for the fabrication of electronic devices. Some of the limitations originate in the implantation process, which is used for doping.

The implantation technique, which is dominating the detector technology, is a very delicate process. It not only introduces the doping atoms into the silicon bulk, but also is a source of impurities and generates crystal defects, which cannot be removed completely. These defects act as generation/recombination centres and therefore are the origin of some noise contribution both in detectors and in the integrated FETs. It is also difficult to tailor sharp doping profiles and control the distribution of dopants due to diffusion during the annealing steps.

To integrate FETs into the detector chips by implantation doping, a number of implants of different energies and ions are necessary [5]. The electrical properties of the FETs are very sensitively depending on the precision of the dose, the energy, the angle of incidents of the ions (channeling effects) and the annealing conditions. Therefore, it is difficult to achieve high reproducibility from one production run to the next.

In addition, the radiation damage which cannot be removed completely, is responsible for random telegraph noise and high  $1/f$  noise of the integrated FETs. The high noise and poor quality of the FETs can only be compensated by the extremely low gate capacitance, which is the reason for the excellent energy resolution achievable with SDDs having integrated FETs [6].

One of the most striking disadvantages of the implantation technique is the fact that the doping is introduced into the detector bulk. This means that the properties of integrated FETs are influenced by the potential distribution within the detector. This effect is very well known from SDDs with integrated FETs, where precise settings of all the detector voltages are mandatory.

In SDD devices with integrated FETs there is a distortion of the electric field below the FET, which results in charge loss [7] and influences the shape of the energy spectrum of X-rays. To avoid

this problem the droplet shaped SDD devices have been designed [6], where the FET is placed at the periphery of the device. The position of the FET outside the active area of the detector is also of advantage in respect to radiation damage, to avoid the worsening of electrical parameters. Additionally the gate area of the FET can be minimized and therefore energy resolution can be improved clearly.

To get rid of all these problems a new technology has been developed for the fabrication of the next generation of sophisticated silicon detectors like SDDs or pixel detectors by replacing the implantation doping by the epitaxial growth of doped silicon layers. Epitaxy is very well established in modern device fabrication as it has a number of advantages compared to implantation doping [8].

Epitaxy enables the fabrication of very shallow highly-doped perfect mono-crystalline layers [8], which can be used as extremely thin entrance windows for radiation detectors without metal contacts. No annealing is necessary and no radiation damage is left within the layers. All types of electronic components, which can be implemented by epitaxy, are located on top of the detector volume, not within the bulk. Therefore, their properties are independent of the operating voltages of the detector and not sensitive to radiation, too.

## 2. Epitaxial deposition technique for radiation detectors

### 2.1. General

Most common deposition techniques for silicon epitaxy are molecular beam epitaxy (MBE) and chemical vapour deposition (CVD). Each of these techniques gives a competitive edge with regard to special applications as summarized in Table 1. With MBE it is possible to fabricate layers in atomic scale, which are needed for quantum well devices and nano-electronics. CVD technology enables fast deposition of layers of excellent homogeneity in thickness as well as in doping concentration, even on large area substrates up to

Table 1  
Comparison of MBE and CVD

	Mechanism	Dep. temp. (°C)	Dep. rate (nm/min)	Application
MBE	Non-thermal equilibrium, controlled by kinetics	450–700	0.1–10	Controlled deposition of ultra thin layers with shallow doping profiles; low dep. temp.
CVD	Near thermal equilibrium	600–1200 (depending on precursor)	10–1000	High dep. rate and excellent homogeneity on large area substrate; low defect density

MBE enables controlled deposition of ultra thin epitaxial layers, while CVD allows fast growing of very homogeneous layers on large area substrates.

300 mm. Since UHV-technology can be avoided it is a production technology suitable for high throughput also within single wafer processing [9]. The achievable doping levels are about  $1 \times 10^{20} \text{ cm}^{-3}$  for boron and  $1 \times 10^{19} \text{ cm}^{-3}$  for phosphorus [8].

## 2.2. CVD-technique for radiation detectors

For the fabrication of high-quality radiation detectors the avoidance of any contamination, causing a reduction of charge carrier life time and with it an increase of leakage current, is ultimate ambition. Within this work low pressure CVD (LPCVD) technique has been chosen: LPCVD technique enables in addition to in situ HCl-cleaning of the quartz glass process chamber the removal of trace contaminants from the silicon surface by formation of volatile halides and metal chlorides, which are transported away by the gas stream. Thus the deposition of epitaxial layers of high purity is possible.

Additionally, selective epitaxial growth (SEG) of silicon by LPCVD using gas systems like  $\text{SiH}_4/\text{HCl}/\text{H}_2$  or  $\text{SiH}_2\text{Cl}_2/\text{HCl}/\text{H}_2$  enables the very efficient fabrication of locally doped areas simply by patterning of a silicon oxide layer. If the epitaxial layer does not exceed a critical thickness, which depends on substrate pre-treatment and process conditions, no poly silicon is deposited on top of the passivating oxide and therefore no additional patterning is required after epitaxy [10].

The presented fabrication process requires three epitaxy steps: (a) deposition of anode, (b) drift and guard structures and (c) entrance window with guard structures. Thus at least three lithography masks can be omitted using SEG, which makes this process very attractive with respect to cost reduction and simplification of the fabrication process for commercial production of detectors. For simple SDDs without integrated electronics only seven mask steps are necessary.

## 3. Experimental procedure

### 3.1. Feasibility study with pin-diodes

The suitability of epitaxy for detector fabrication was tested first by comparing the leakage currents of  $\text{p}^+\text{-n}$ -entrance window structures of an active area size of  $10 \text{ mm}^2$  fabricated by implantation doping with those fabricated by epitaxy using the standard process line for electronic devices at the Physics Institute of the University of the German Federal Armed Forces at Munich. The wafers used were of (100) orientation and n-type with a resistivity of about  $3 \text{ k}\Omega\text{cm}$ . The thickness was  $300 \mu\text{m}$  and the diameter  $100 \text{ mm}$ . The thermal oxidation process was identical for the differently processed wafers. After oxide etching the  $\text{p}^+$ -doping was carried out in two different ways: (a) boron implantation (30 keV) through an about  $120 \text{ nm}$  thick oxide window for the 'implanted' wafers and (b) deposition of boron doped thin

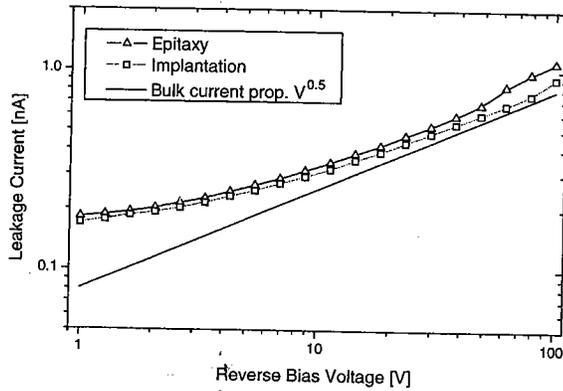


Fig. 1. Comparison of leakage currents of  $p^+n$ -entrance window structures ( $10\text{mm}^2$  active area), fabricated on high resistive substrate material ( $3\text{k}\Omega\text{cm}$ ) by implantation doping and epitaxial deposition, respectively. In both cases the main contribution results from bulk current.

epitaxial layers into the free windows using a single wafer industrial CVD-epi-reactor for the ‘epi’-wafers. After deposition of metal pads both entrance window structures have been tested.

Typical results of  $I/V$  measurements are plotted in Fig. 1. In both cases the leakage currents are in the same range of approximately  $1\text{ nA}$  at  $100\text{ V}$  bias at room temperature and are determined by the bulk current. Though these very first results achieved in a standard process line cannot yet compete with best values obtained after 25 years of optimization of implantation detector technology, they show that epitaxy can replace the implantation doping without fearing any drawbacks in leakage currents. In contrast it is expected that even lower leakage currents can be achieved with epitaxy than by implantation doping after optimization of the individual process steps due to the before mentioned benefits of epitaxy.

### 3.2. Fabrication of the first SDDs with epitaxy

A schematic cross section of the SDDs fabricated by LPCVD epitaxy is shown in Fig. 2. SDDs need  $p^+n$ -junctions on both sides and an additional  $n^+$ -contact for the anode on the drift side [3]. Both the  $p^+n$ -junctions and the  $n^+$ -contact are fabricated by SEG. To generate a suitable drift

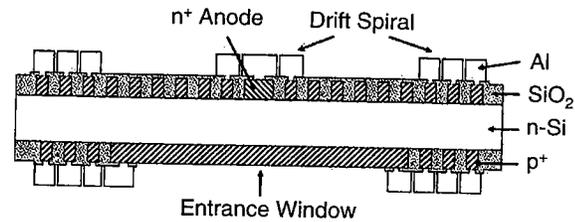


Fig. 2. Schematic cross section of the SDD, using SEG instead of implantation doping.

field a resistive spiral was designed with the anode in the centre. The radial potential gradient can be adjusted by varying the width of the conducting path. The complete resistivity of the drift field generating spiral can be tuned by proper selection of the thickness and the doping concentration of the epitaxial layer.

The process flow chart of the detector fabrication using epitaxy is shown in Fig. 3. After thermal oxidation the anode area at the drift side is opened by wet chemical oxide etching. In a consecutive SEG process a  $n^+$ -doped epi-layer of  $50\text{ nm}$  thickness is deposited. After that a thin thermal oxide is grown on top of the anode to prevent further deposition within the next SEG processes.

The remaining  $p^+n$ -junctions of drift field spiral and entrance window are generated in two back-to-back steps of oxide structuring and boron doped SEG-processing. Subsequently, all epitaxial silicon areas are passivated by oxide. Finally the contact holes are opened and the AlSi metallization is deposited and patterned on both wafer sides to enable contacting by ultrasonic wire bonding.

The thickness of the  $p^+$ -epi-layer at the entrance window is  $75\text{ nm}$ , which is about a factor 4 higher compared to the thickness of implanted windows [11]. In contrast to the implanted window the epi window has not been covered by an aluminium layer. However, the epitaxy has the potential to reduce the window thickness down to several  $\text{nm}$ , which makes this technique superior over implantation and very attractive for low energy X-ray detectors. Moreover, the epitaxy technique allows very sharp doping distributions compared to the implantation technique.

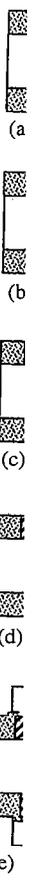


Fig. 3. (a) anode, oxide and oxide.

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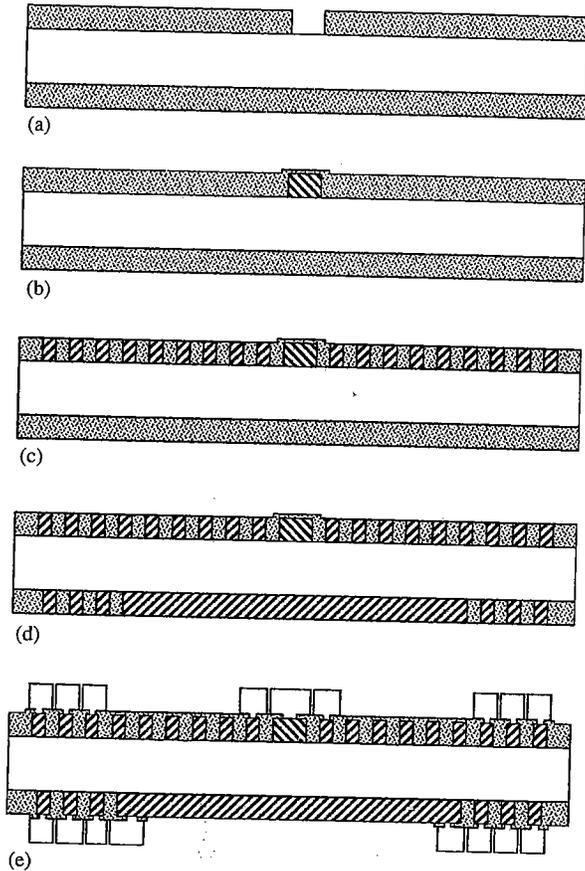


Fig. 3. Process flow chart of the SDD detector using SEG: (a) oxide growth and oxide patterning (Mask 1), (b) n-SEG of anode and growth of passivation oxide layer, (c) patterning of oxide and p-SEG of drift spirals (Mask 2), (d) patterning of oxide and p-SEG of entrance window (Mask 3), (e) growth of passivation oxide, patterning of oxide and metallization (Mask 4...7).

#### 4. Experimental results

##### 4.1. Static tests of the SDD devices

To generate a constant drift field a spiral was designed, which shows increasing width from the centre to the periphery as can be seen from Fig. 4. By choosing a thickness of 75 nm and a doping concentration of  $3 \times 10^{19} \text{ cm}^{-3}$  of boron, the overall resistance of the spiral is about 1.25 M $\Omega$  for the 10 mm<sup>2</sup> detectors. The excellent linearity of the drift spirals is demonstrated in Fig. 5, while Fig. 6

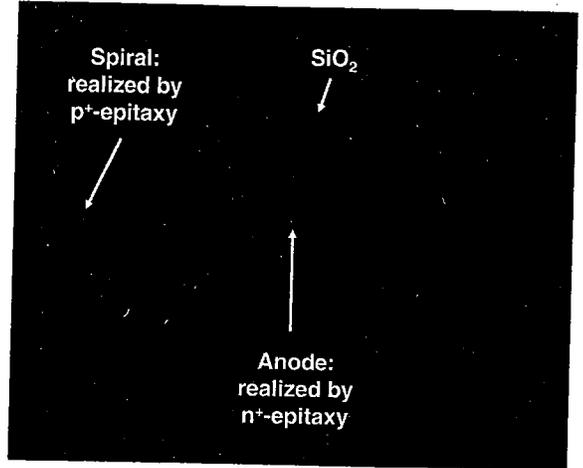


Fig. 4. SEM picture of the spiral shaped resistive voltage divider and the readout anode.

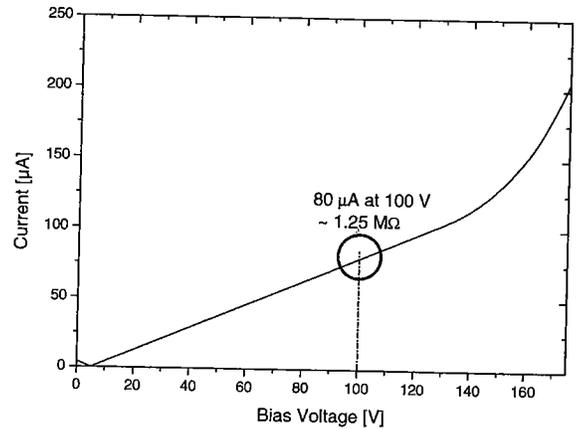


Fig. 5. Test of the voltage divider shows a perfect linearity up to 130 V. At a voltage of 100 V the current is about 80  $\mu\text{A}$  which gives a resistance of 1.25 M $\Omega$ .

shows the radial potential distribution of the drift spiral for different voltages at the last spiral winding. The innermost contact is forced to 0 V. The drift spiral is designed in a way to produce an exact linear potential.

The behaviour of the leakage currents of the devices is identical with those of Fig. 1. At a reverse bias of 100 V the currents are about 1 nA at room temperature for detectors with an area of 10 mm<sup>2</sup> and a thickness of 300  $\mu\text{m}$ .

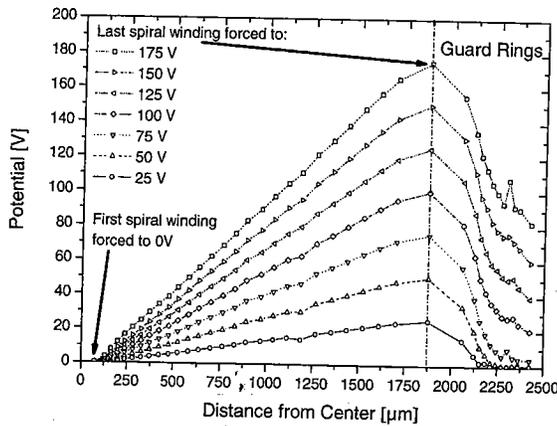


Fig. 6. Radial potential distribution of the drift spiral for different voltages at the outer contact of the spiral. The innermost contact is forced to 0V. The potential shows an excellent linearity even for high voltages up to 175 V at the outer contact.

For qualification of SDDs the anode current is an important measure. The anode current can be determined by contacting the anode directly with a needle probe. All detector voltages can be applied during this measurement besides the back voltage. Nevertheless a complete depletion of the whole detector volume can be achieved by applying two times the depletion voltage at the outermost ring. For good detectors anode current values have to stay below 1 nA at room temperature. The plot of Fig. 7 shows the dependence of the anode current on temperature. At room temperature the value is about 500 pA. By cooling of the device the anode current can be reduced by a factor of 2 every 7°. This is the typical behaviour of a bulk generation current.

#### 4.2. Spectroscopic tests with $^{55}\text{Fe}$ source

For spectroscopic tests the SDD devices have been mounted into the standard detector housings developed lately for SDD chips, which are operated with external FETs using the pulsed reset technique. This technique is an approved method in combination with SiLi-detectors for example. Within the housing the chip is glued on a ceramic substrate which is mounted on a thermoelectric cooler. The irradiated area of the detector

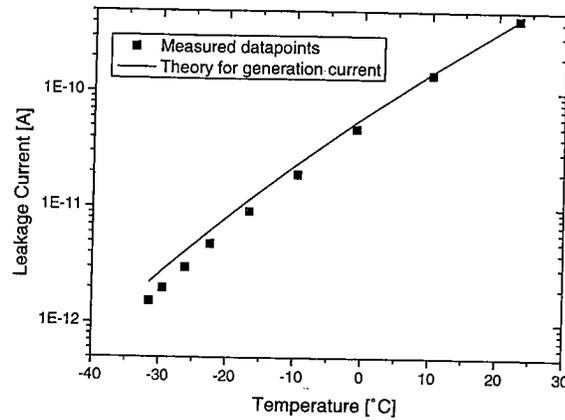


Fig. 7. Temperature dependence of the anode current measured with the help of the reset frequency of the pulsed reset. The behaviour follows the prediction for the generation current.

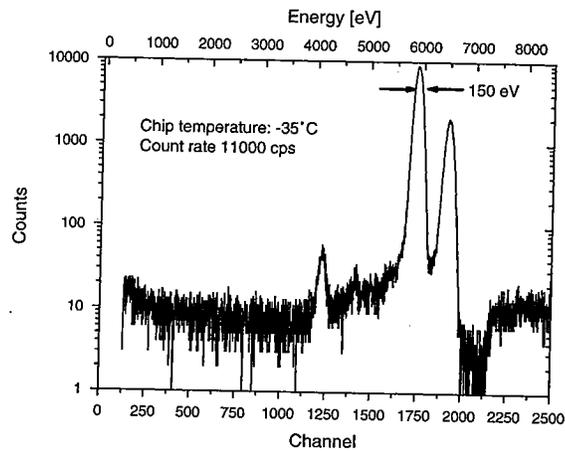


Fig. 8. Typical energy spectrum taken with an epitaxial SDD at  $-35^\circ\text{C}$ . FWHM energy resolution is 150 eV at a shaping time of 1.5  $\mu\text{s}$ . Peak to background value is 900 when irradiating the whole chip with an on-chip collimator with an area of 10  $\text{mm}^2$ .

(10  $\text{mm}^2$ ) is defined by the on-chip collimator, which is fixed on the entrance window of the SDD. The electronic components are assembled at the rear side of the chip.

Several tests with a  $^{55}\text{Fe}$  source have been performed at different temperatures by irradiation of the whole area of the detectors and by application of collimators to shield the rim of the devices. A typical energy spectrum is plotted in Fig. 8. At a temperature of  $-35^\circ\text{C}$  and a shaping

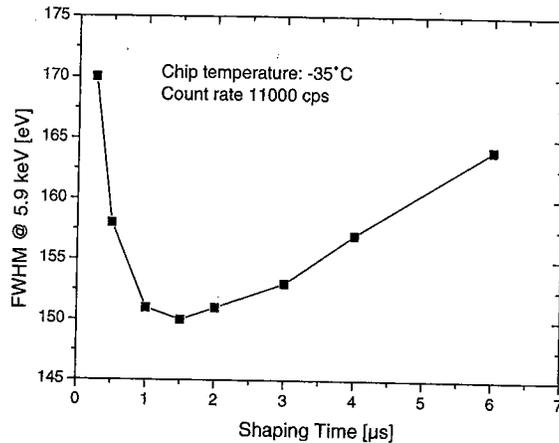


Fig. 9. FWHM energy resolution versus shaping time at a temperature of  $-35^{\circ}\text{C}$ . The best energy resolution can be achieved at a shaping time of  $1.5\ \mu\text{s}$ . For longer shaping times the contribution due to the leakage current is increasing.

time of  $1.5\ \mu\text{s}$  a FWHM of  $150\ \text{eV}$  for the Mn  $K_{\alpha}$ -line could be achieved, which is still determined by the leakage current, however, already comparable to the values of good quality standard SDDs.

Detector voltages were  $-47\ \text{V}$  for the back voltage,  $-100\ \text{V}$  for the outer contact of the spiral and  $-4.5\ \text{V}$  for the inner contact of the drift spiral. A current of  $57\ \mu\text{A}$  is flowing in the spiral. Count rate was relatively high with  $11,000$  counts per second. For the pulsed reset technique the count rate dependence of the FWHM is negligible for count rates up to  $50,000\ \text{cps}$ .

Fig. 9 shows the dependence of the FWHM on the shaping time of the preamplifier. It becomes apparent that the charge collection within the SDD devices is perfect over the whole area and that within a broad range of shaping times the devices are operating fine. One can also see that for longer shaping times energy resolution gets worse which is a characteristic behaviour for detector leakage current. The optimum shaping time is  $1.5\ \mu\text{s}$  for the chosen detector which allows high count rate applications.

## 5. Discussion and future perspectives of epitaxy

The good spectroscopic results obtained with the very first SDD devices ever fabricated in a

standard process line for electronic devices by application of epitaxy instead of implantation doping demonstrate the high potential of this new technology for future detector generations.

First of all it is possible to fabricate very shallow highly-doped entrance windows of perfect crystal quality for low energy X-ray detectors, which are radiation hard and do not need any additional metal contacts. The practical limit in thickness is around  $10\ \text{nm}$  for LPCVD and below  $1\ \text{nm}$  for MBE. The effective window thickness can be reduced, alternatively, by an additional doping gradient within the epitaxial layer. Studies for reduction of the effective window thickness are under way and will be presented in near future.

As demonstrated by the drift spiral the epitaxy has the great advantage over implantation in respect of precise tailoring of resistive monocrystalline layers and thus makes the generation of the drift fields very simple and in combination with SEG reduces costs of fabrication of SDDs.

However, the greatest benefit of the epitaxial technology is its high potential for implementation of electronic devices, which can be fabricated by additional epi-layers on top of the detector. FETs of highest quality are commonly fabricated by epitaxy. By integration of the FETs and reduction of the gate capacitance an improvement of the energy resolution for the new generation of SDDs with integrated epitaxial FETs is expected.

The technology is compatible with the processes for fabrication of nano-electronics even in vertical geometry by additional use of MBE [12]. So the door is open now for micro-systems, which combine advanced detectors with a high level of integration of complex electronic circuits. As the electronic components are deposited on top of the active detector volume any influence of the detector on the electronics and vice versa is avoided. Thus, future devices fabricated by epitaxy will not only show excellent spectroscopic behaviour but also long term stability and radiation hardness.

As by epitaxy consecutive mono-crystalline layers of different dopings and thicknesses can be fabricated the realization of some interesting old ideas [13] is now possible. This concerns e.g.  $dE/E$  detectors and detector telescopes for heavy ions,

wave length sensitive monolithic detector stacks and three dimensional CCDs.

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