Title	***Booster FPGA-Based Ramp Correction***			
Project Requestor	Michael Borland			
Date	March 21, 2008			
Group Leader(s)	Arnold, Borland, Wang			
Machine or Sector Manager	Nicholas Sereno			
Category	Accelerator Hardware and ID Improvements			
Content ID*	APS_XXXXXX	Rev.	ICMS_Revision	ICMS Document Date

*This row is filled in automatically on check in to ICMS. See Note [1]

Description:

Start Year (FY)	**2009**	**Duration (Yr)**	**3**

Objectives:

The purpose of this initiative is to improve tunability, day-to-day reproducibility, and shot-to-shot performance for the booster. This will be accomplished by improving the ramp correction system by incorporating the functions of the programs "Bcontrol" and "fixramp" into the FPGA algorithm.

Benefit:

Smoother operation with more tolerance for upstream errors and more consistent delivery of beam to the storage ring for top-up.

Risks of Project: See Note [2]

Low.

Consequences of Not Doing Project: See Note [3]

Continued intermittent problems with booster performance.

Cost/Benefit Analysis: See Note [4]

The components of this initiative are not costly, yet the benefits can be significant.

Hence, the cost/benefit is favorable.

Description:

A description of this proposal in the context of an overall Booster improvement plan is available in OAG-TN-2008-008, Section 3.

FPGA's are a modern technique for implementing fast digital acquisition and control. Recently, an FPGA-based tune measurement system was built for the booster. We propose to build on this success and develop FPGA-based ramp correction for the booster main power supplies to replace the existing slow software-based system. This would stabilize shot-to-shot performance and perhaps allow injecting at lower energy. The former is important for reliable top-up and uniform filling of buckets, while the latter helps to decrease demands on the upstream injector, particularly the linac. Input from the tune measurement system may be useful in automatic ramp correction. Six FPGA's and one Taxi board would need to be purchased (1 FPGA for each ramping supply and 1 spare).

Funding Details

Cost: ($K)
Use FY08 dollars

Strategic Project Proposal

Funding Details
FY 08 $

Cost ($k)

Year	AIP	Contingency
1	25	10.00%
2		
3		
4		
5		
6		
7		
8		
9		
Total	25	

Contingency may be in dollars or Percent

The effort portion need not be filled out in detail by March 28

Effort (FTE)

Year	Mechanical Engineer	Electrical Engineer	Physicist	Software Engineer	Tech	Designer	Post Doc	Total
1		0.33	0.33	0.33				0.99
2								0
3								0
4								0
5								0
6								0
7								0
8								0
9								0

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[1] **Notes:**

ICMS. Check in first revision to ICMS as a *New Check In*. Subsequent revisions should be checked in as revisions to that document i.e. C*heck Out* the previous version and C*heck In* the new version. Be sure to complete the *Document Date* field on the check in screen.

[2] **Risk Assessment.** Advise of the potential impact to the facility or operations that may result as a consequence of performing the proposed activity. Example: If the proposed project is undertaken then other systems impacted by the work
include ... (If no assessment is appropriate then enter NA.)

[3] **Consequence Assessment.** Advise of the potential consequences to the facility or to operations if the proposal is not executed. Example: If the proposed project is not undertaken then ____ may happen to the
facility. (If no assessment is appropriate then enter NA.)

[4] **Cost Benefit Analysis.** Describe cost efficiencies or value of the risk mitigated by the expenditure.
Example: Failure to complete this maintenance project will result in increased total costs to the APS for emergency repairs and this investment of ___ will also result in improved reliability of ____. (If no assessment is appropriate then enter NA.)